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Reversible Full Adder Design with Reduced Quantum Cost

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ABSTRACT: The reversible logic is the most prominent logic design for low power circuit design having its applications in low power CMOS, quantum computing, nano technology and optical computing. it has equal number of inputs and outputs, it has property that input is uniquely constructed by the outputs. The basic reversible logic gates are used to design the 16 bit carry look ahead adder and carry skip adder, the basic gates used are fredkin gate, New fault tolerant gate and Feynman gate as conventional gates looses information and each missing information looses kTlog2 joules/bit information, Reversible gates have inertia to correct the missing information due to one-one mapping from input to output we have design 16 bit adder with minimum quantum cost. It means minimum number of 2*2 reversible gates to design the whole circuit of full adder, Any reversible logic gates is designed with NOT gate , Controlled (-V) gate and Controlled(+V) gate, the number of these elements are used to construct a reversible gate is generally called as quantum cost of the reversible gate, we have proposed a 16 bit adder with minimum quantum cost and is simulated in xilinx 9.1i using verilog code delay in carry skip adder and carry look ahead adder is 27ns and 40 ns with power loss of 24 and 48 uW the quantum cost of CLA(carry look ahead adder) is 254 and 340 for CSA(carry skip adder.

I. INTRODUCTION

The energy-efficient digital signal processors (DSPs) are becoming increasingly important in wireless sensor networks, where tens to thousands of battery-operated micro sensor nodes are deployed remotely and used lo relay sensing data to the end-user. Given the constantly changing environments of portable devices and the extreme constraints on battery lifetimes, power-saver design considerations should be taken into account.

Many wireless sensor network applications involve complex digital signal processing (DSP) of gathered data and implementation of a protocol stack. A power-saver DSP module will be able to adapt energy consumption as energy resources of the system diminish or as performance requirements change. Therefore it is advantageous to design the power-saver DSP module with power scalability hooks such as variable bit-precision and variable memory size so that it can be used for a variety of scenarios and changing operating conditions of each individual sensor node.

Breakthroughs in low-power technologies are extending running times for portable devices employing media processing and communication applications. To accomplish these applications, many researchers have proposed advanced low-power techniques at the algorithm level, system level, architecture level, circuit design level, and fabrication process level. The algorithm of a specified application can be modified to compromise algorithmic performances with computational complexity. Reversible logic is likely to be in demand in high speed power aware circuits since they do not erase (lose) information and dissipate very less heat. Reversible logic can be of prominent interest to design low power arithmetic and data path units for digital signal processing applications, such as the designs of low power adders, multipliers, FFT, IDCT etc, and quantum computers. Quantum logic gates perform an elementary unitary operation and any unitary operation is reversible, hence quantum networks effecting elementary arithmetic operations must be built from reversible logic components. Thus, reversible logic will also be the immediate requirement to solve DSP problems with quantum computers.

Reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping between input and output vectors.

It has been shown that for irreversible logic computations, each bit of information lost generates kTln2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed, since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Furthermore, voltage-coded logic signals have energy of Esig= ½CV2, and this energy gets dissipated whenever switching occurs in conventional (irreversible) logic implemented in modern CMOS technology. It has been shown that reversible logic helps in saving this energy using charge recovery process. The most prominent application of reversible logic lies in quantum computers.

A quantum computer will be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates; each gate performing an elementary unitary operation on one, two or more two–state quantum systems called qu-bits. Each qu bit represents an elementary unit of information; corresponding to the classical bit values 0 and 1. Any unitary operation is reversible and hence quantum networks effecting elementary arithmetic operations such as addition, multiplication and exponentiation cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible).Thus, quantum arithmetic must be built from reversible logical components.

II. FUNDAMENTAL LOGIC GATES

There are three types of fundamental 2*2 reversible logic gates. First, the square-root-of-not gates utilize the unitary operators to produce reversible logic calculations. The Controlled-V and the Controlled-V+ gates are the two types of square-root-of-not gates. In both of these gates, when the control input is 0, the second input is propagated to the output. The corresponding unitary operator is propagated to the second output when the control input is 1, where the unitary operation is V= $\frac{t+1}{2}\begin{pmatrix}1 & -i\\ -i & 1\end{pmatrix}$ for the Controlled-V gate and is V+ = $\frac{t+1}{2}\begin{pmatrix}1 & -1/i\\ -i & 1\end{pmatrix}$ for the Controlled-V+ gate. When two Controlled-V gates are activated in series, they act as an inverter. The same holds for two Controlled-V+ gates in series. When a Controlled-V and Controlled-V+ gate are activated in series, they act as an identity.

The second type of fundamental 2*2 reversible-logic gate is the Feynman gate Fig 1, or the Controlled-Not gate. Proposed by Feynman, it is configured such that its outputs states correlate to the input states in the following manner:

P= A & Q=A XOR B

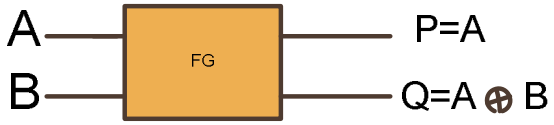


Fig.1. Feynman logic gates.

The resulting value of the second output corresponds to the result of a conventional XOR gate. Since fan-out is expressively forbidden in reversible logic, since a fan-out has one input and two outputs, the Feynman gate may be used to duplicate a signal when B is equal to 0. Its quantum configuration is shown in fig 2

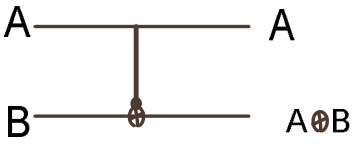


Fig 2. Quantum Representation of Feynman gate.

The third type of fundamental 2*2 reversible logic gate is the integrated qubit gate. This gate is implemented with a Feynman gate with either a Controlled-V or Controlled V+ gate. The XOR output of the Feynman gate is used as the control signal for the Controlled-V or V+ gate it is coupled with. The quantum cost of the integrated qubit gate is 1 and its worst-case delay is 1. The quantum configurations of these gates are shown below in Fig.3.

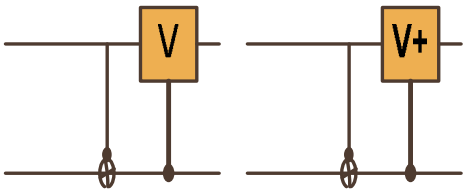


Fig. 3. Quantum Representations of Integrated Qubit Gates.

There are three 3*3 fundamental reversible logic gates. The first was proposed by Fredkin and Toffoli. The Fredkin gate's outputs states map to the inputs as follows:

P=A, Q=A'B+ AC and R = AB + A'C. (Fig 4)

Therefore, the outputs serve as a multiplexed output of the two data inputs based on the control input. It is realized using 2 Feynman gates, a Controlled-V gate and two integrated qubit gates. Toffoli proposed the second fundamental 3*3 reversible logic gate. The output states of the Toffoli gate map the inputs in this manner:

P = A, Q =B, And R = AB XOR C.
The quantum cost is 5 and the worst-case delay is 5. The quantum representation is shown below in Fig.4

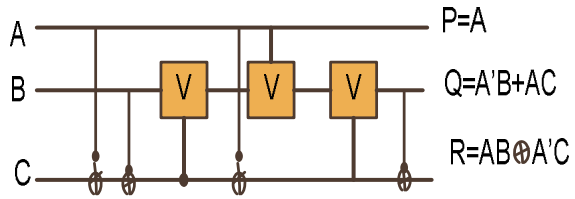


Fig. 4. Quantum Representation of Fredkin gate.

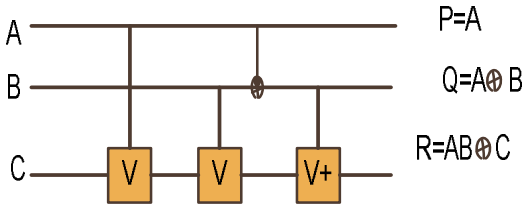


Fig. 5. Quantum Representation of Toffoli gate.

The 3*3 Peres gate was proposed by Peres. The Peres gate has a quantum cost of 4 and a worst-case delay of 3. The quantum representation is shown in Fig 6 The output states map to the inputs in this manner:

P = A, Q = A XOR B, and R = AB XOR C,

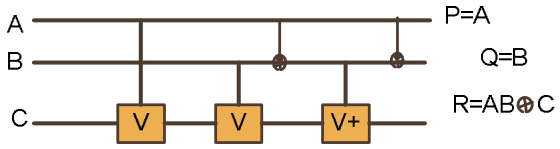


Fig. 6. Quantum Representation of Peres gate.

The 3*3 New Fault Tolerant gate (NFT) with quantum cost of 5 is shown in fig.7 has worst case delay of 3 it has better correction capability. The output states map to the inputs in this manner:

P = A XOR B, Q = AC' XOR B'C, and
R = AC' XORB C,

The 3*3 Feynman double gate gate with quantum cost of 2 is shown in fig. 8. has worst case delay of 3 it has better correction capability

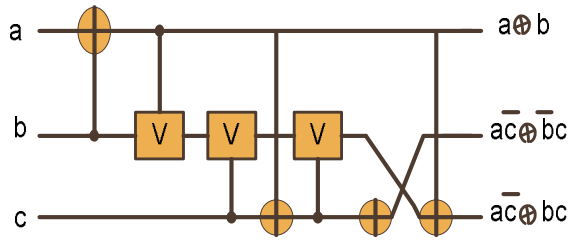


Fig. 7. Quantum Representation of NFT gate.

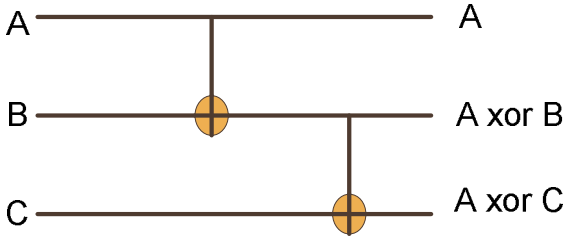


Fig. 8. Quantum Representation of F2G gate.

III. PROPOSED DESIGN

The proposed design of cost effective Reversible Fault Tolerant Full Adder by using New Fault Tolerant (NFT) and Feynman Double (F2G) gates. Then we have described the design of Fault Tolerant Carry Skip (RFT-CSA) and Carry Look-ahead (RFT-CLA) adders by using proposed design of Fault Tolerant Full Adder

Single NFT Full Adder (SNFA) is a Fault Tolerant full adder circuit which consists of one New Fault Tolerant (NFT) gate and three Feynman Double (F2G) gates where the quantum cost is 11 and the total number of garbage output is 3 (shown in Fig. 9). The minimum number of garbage bit to realize Reversible Fault Tolerant Full Adder circuit is 3.

And proved as Let, a, b and $_{cin}$ are the inputs of a full adder circuit where s and $_{cout}$ are the corresponding outputs. There are three different states at the inputs (a, b and $_{cin)}$ where the outputs (s and $_{cout)}$ produce same patterns as shown in Table II. For any parity preserving reversible circuit, total number of EVEN or ODD parity at input or output is equal. Table II shows that the all input patterns are EVEN but the corresponding output patterns are ODD. Turning three ODD patterns at output into EVEN by adding two extra bits is not possible. Because two bits can represent 2^2 different states where 00 and 11 (01 and 10) are EVEN (ODD) only. So, Reversible Full Adder circuit requires at least 3 garbage bits to make itself Reversible Fault Tolerant Full Adder

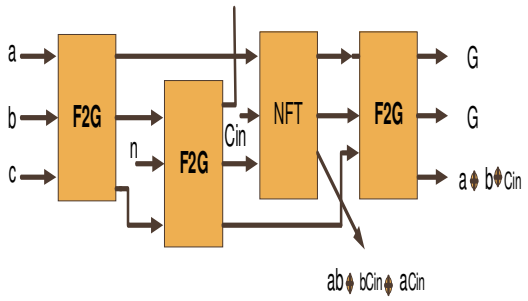


Fig. 9. Proposed design of Fault Tolerant single NFT Full Adder (SNFA).

A. Design of N-bit RFT-CSA (n+5) F2Gs, n FRGs and n NFTs

N-bit RFT-CSA can be realized with (n+5) Critical Path Delay. The proposed design of 4-bit RFT-CSA is shown in Fig. 10 which uses proposed full adder (SNFA) circuit. Finally, the total garbage (GBCSA) and Quantum Cost (QCCSA) of n-bit RFT-CSA can be written as follows:

$GB_{CSA} = 4n$

$QC_{CSA} = 5*2n + 2*(3n + 1)$

$= 16n + 2$

Carry Skip Adder is more reliable in case of hardware implementation where circuit cost is another factor of design with respect to Delay. The QC of proposed design is 66 which is minimum than all existing designs. Although the number of 3×3 gates of [7] is about equal to proposed design but QC of proposed design has been improved 20% because of using cost effective Feynman Double gate (QC of Feynman Double gate is only 2). The proposed cost-effective design of Fault Tolerant CSA (RFT- CSA) has improved cost factor having fault detection as well. Fig. 11 shows 16 bit RFT- CSA

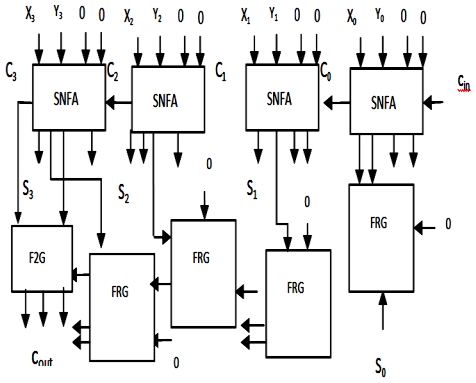


Fig. 10. Proposed design of Reversible Fault Tolerant Carry Skip Adder with 16 garbage values.

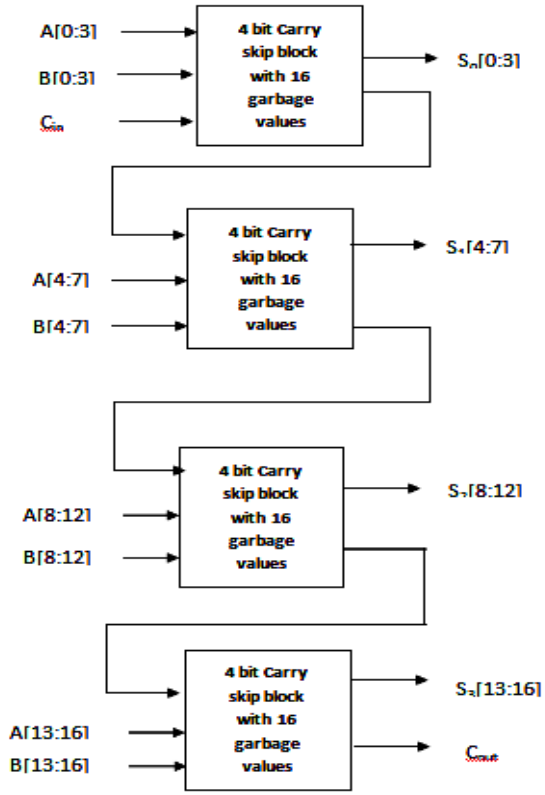


Fig. 11. Proposed design of Reversible Fault Tolerant Carry Skip Adder with 16 garbage values.

This section introduces the design of Reversible Fault Tolerant Carry Look-ahead Adder (RFT-CLA) circuit overlaps the performance of all existing designs. Proposed design of RFT- CLA is based on New Fault Tolerant (NFT) and Feynman Double (F2G) gates where the carry is generated before sum. Reversible Fault Tolerant Carry Look ahead Adder (RFT-CLA) consists of serial attachment of n SNFAs but the work as a carry generator itself where the carry output of ith stage (ci) is produced before sum si where i= 0, 1, 2, ..., (n-1).n-bit RFT-CLA can be realized by using the combination of n NFTs and n F2Gs as shown in fig 12. The Delay of n-bit Reversible Fault Tolerant CLA (DRF T -CLA) can be minimized to (n+3). Proved as, the Delay of any circuit is the number of maximum gates laying on contiguous path of any input to output. The Delay of SNFA, DSNF A= 4 to generate sum not carry.

B. Fault Tolerant Carry Look-ahead Adder Circuit

Delay of parallel adder circuit depends on carry propagation (from c_{in} to c_{out}) of every stage. Any n-bits RFT-CLA needs n SNFAs where Delay of RFT- CLA, DRF T -FA_= 4n.

Because carry input (ci) of ith stage is generated by spending 1 units Delay where i= 0, 1, 2, ..., (n-1). In first stage, extra two units Delay is added because of first carry output (c0) generation is related to operands at first stage. On the other hand, last stage has extra single unit Delay because the final sum is generated after one stage of generation of final carry (cout). So the Delay calculation for n-bits RFT-CLA is as follows:

$D_{RFT-FA} = n + 3$

and fig. 13 shows 16 bit RFT- CLA

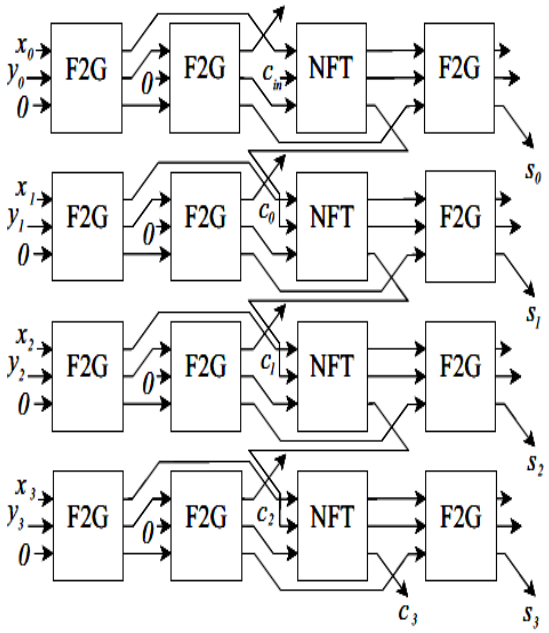


Fig. 12. Proposed design of Reversible Fault Tolerant Carry Look ahead Adder with 12 garbage values.

IV. SIMULATION RESULT

The above circuit is simulated in Xilinx 9.1i using Spartan 3 series the delay in carry skip adder and carry look ahead adder is 27ns and 40 ns with power loss of 24 and 48 uW the quantum cost of CLA(carry look ahead adder) is 254 and 340 for CSA(carry skip adder a table 1. shows the comparison with the other techniques of reversible logic to design the adder circuit. The simulation result were shown in fig14,15,16,17 and table 1 shows comparison between CLA & CSA adder table 2 shows comparison with previous work, and table 3 shows comparison in between CLA & CSA with respect to no, of gates, garbage output, delay and quantum cost.

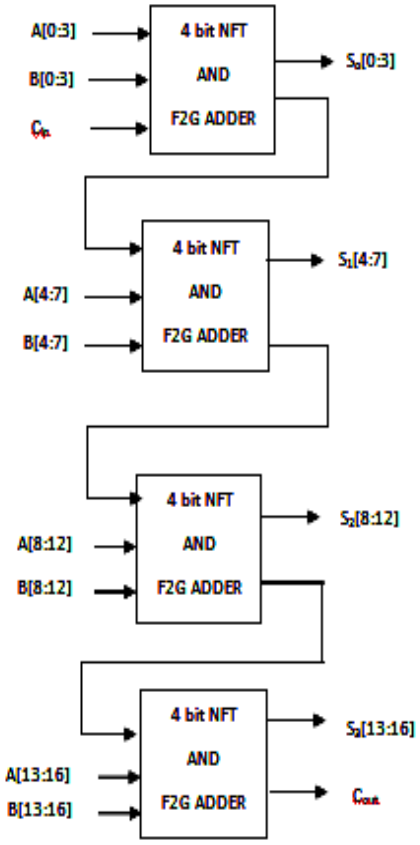


Fig. 13. Efficient Design of 16- Reversible Fault Tolerant Carry Look-ahead Adder bit.

V. FUTURE WORK

Now a day accuracy is the main goal to achieve with this fast processing environment and it will also consumes less energy , previous conventional circuits are non reversible and due to which during communication of data when there is loss of information circuit dissipates energy due to reload of data in between communication channel from input to output vectors. As reversibility recovers energy loss and prevent bit error by including fault tolerant mechanism. It is gaining much popularity in quantum computing, CMOS technology and DNA informatics. Now the main aim towards this technology is to achieve fault tolerant system and with increased speed So we have to make a circuit under optimized way in manner that it will be cost effective in the sense of Gate cost, delay, garbage and quantum cost taking all these in account we have to design the optimized circuit which are reversible and have capability to detect and correct the error during data transmission.

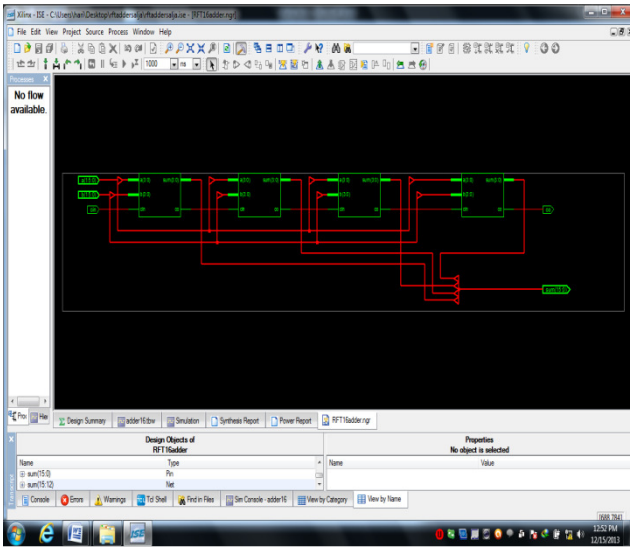


Fig 14. Expandable Block diagram of 16 bit CLA adder using NFT & F2G.

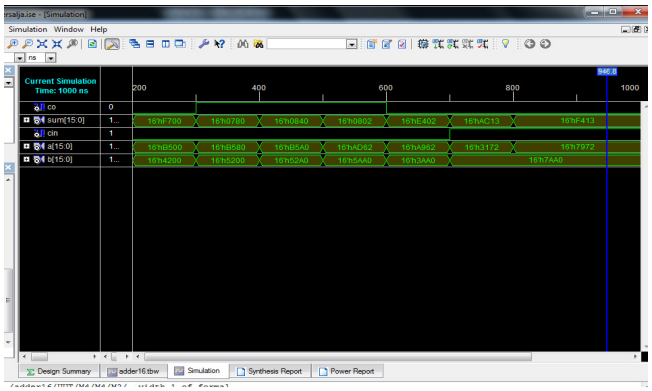


Fig. 15. Simulation result of 16 bit fault tolerant CLA adder.

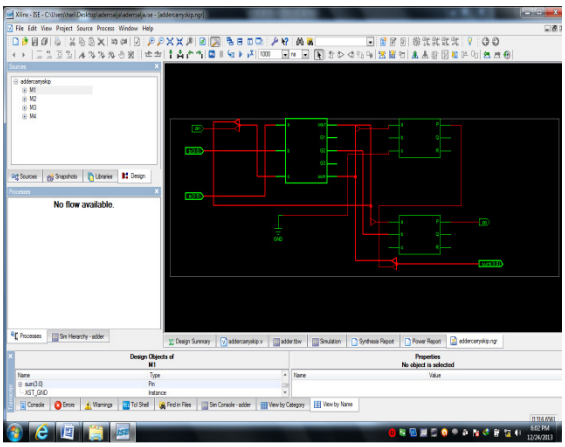


Fig. 16. Expandable Block diagram of 4 bit CSA adder using NFT, FRG & F2G.

Table 1: Comparison in between CLA & CSA.

ADDER TYPES	CLA ADDER	CSA ADDER
VENDOR	XILINX	XILINX
DEVICE AND FAMILY	Spartan 3	Spartan 3
POWER DISSIPATION	24mW	38mW
ESTIMATED DELAY	28ns	40ns

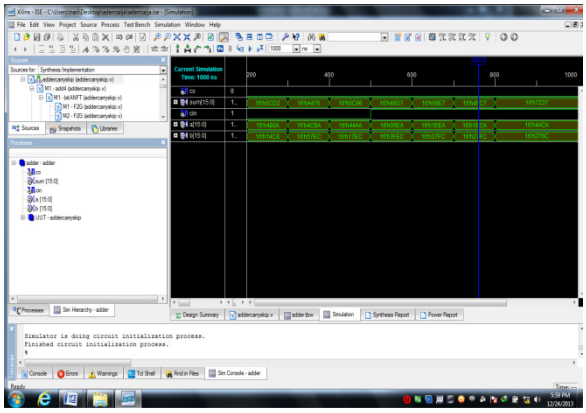


Fig. 17. Simulation result of 16 bit fault tolerant CLA adder.

Table 2: Comparison table between Proposed work, [7,8,9] of CLA ADDER.

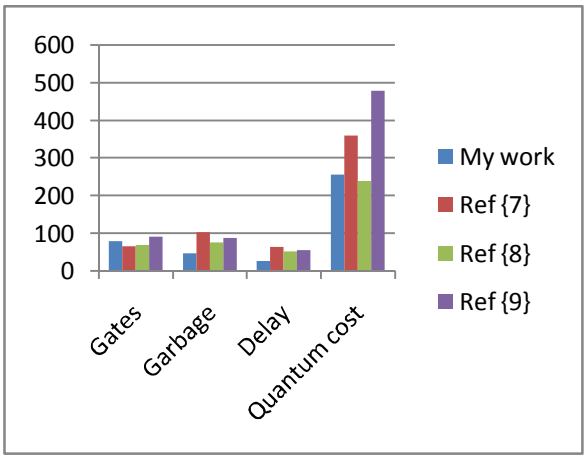
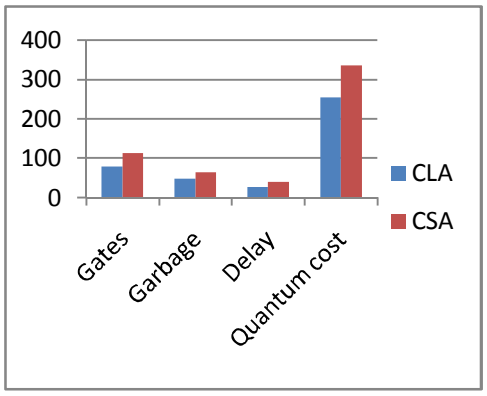


Table 3: Comparison table between CLA & CSA.



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