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The Design and Implementation Of Single Stage Zero Voltage Switching Converter With Boost Type Active Clamp

Prabodh Khampariya, Md. Ashfaque Khan and Dr. Amita Mahor

Department of Electrical & Electronics Engineering,

NIIST, Bhopal, (MP)

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ABSTRACT: A predictive boost converter topology with Power Factor Correction (PFC) is presented in this paper that utilizes zero voltage switching to achieve the desired objective. The duty cycle required to achieve unity power factor in one line period integrating input current shaper feature with the AC-DC converter. Simple DC link voltage feedback scheme applied in conjunction with two active clamp switches, where a resonant voltage rectifier helps the output diode to achieve zero current switch operation. The DC link capacitor voltage can be is reduced providing reduced Voltage stress of switching devices. The performance of proposed converter is evaluated for a 160W (48V/3.5A) load and the proposed converter complies with International Electro technical Commission IEC (1000-3-2).

KEYWORD: Boost Converter, PFC, PWM.

I. INTRODUCTION

Boost Converter topology has been extensively used in the various AC/DC and DC/DC Applications. PFC Converter has continued to be key area of research in Power Electronics. These AC/DC converters provide stable DC Voltage at the output with good input Power factor.

Generally, Reduction of reverse recovery losses and EMC problems requires the Boost Rectifier to be softly switch off which is achieved by controlling the device current turn off rate.

A number of soft switched Boost converters and their variation have been proposed [3]-[7], although passive lossless snubber can marginally improve efficiency, their performance is not good enough to make them variable candidates for application in high performance PFC circuit. Generally, they suffer from increased components stress and are not able to operate for soft switching.

The new converter satisfies the input harmonics current limits required by IEC (1000-3-2) and also has fast output response. A centre-tap transformer is employed in the proposed converter the additional winding in the primary side is known as a reset winding in the for word type converter.

A. Proposed PFC Boost Converter:

The present work deals with a high-efficiency single-stage soft-switching converter for universal line voltage applications with a boost type of active-clamp circuit used to achieve ZVS operation of the power switches. The proposed forward AC/DC converter with harmonic current elimination and fast output regulations speed the proposed circuit is an active clamp switch S1 & S2.

The single stage soft-switching converter with boost type of active clamp circuit adopted for validation and analysis for the present work is based on the ZVS topology [15]. The various components of the converter topology are explained below.

II. UNIVERSAL BRIDGE RECTIFIER

The universal diode rectifier bridge fed from a stiff AC power source at 230Vrms acts as fundamental converter with the parameters as indicated in Table 1. The output voltage at the rectifier terminals given by,

$$V_0 = \frac{1}{\pi}\int_0^{\pi} Sin\omega t\, d\omega t \qquad ...1$$

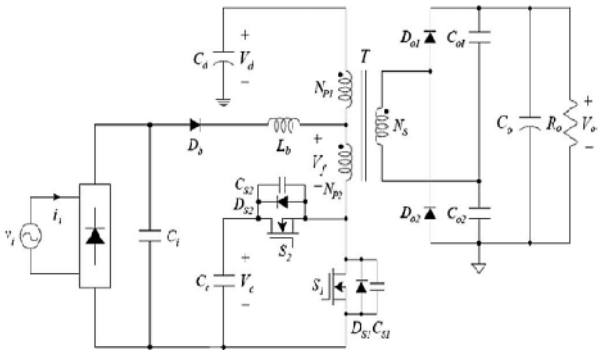


Fig. 1. Circuit diagram of proposed single stage soft switching converter.

Table 1: Rectifier Parameters.

Snubber Resistance (Ohms)	Snubber Capacitance (F)	Ron (Ohms)	Forward voltage drop (Volts)
1e5	1.3e-9	1e-3	0.7

III. ACTIVE CLAMP CIRCUIT

The active-clamp circuit consists of the auxiliary switch S2 and clamp capacitor Cc in parallel with the main switch S1. The output capacitors of the switches S1 and S2 are CS1 and CS2 (CS = CS1 = CS2), respectively. The switch voltages VS1 and VS2 can be clamped to the clamp voltage Vc of the capacitor Cc. The active-clamp circuit is of boost type so that $Vc > Vd$. ZVS operation of the switches reduces the switching power losses.

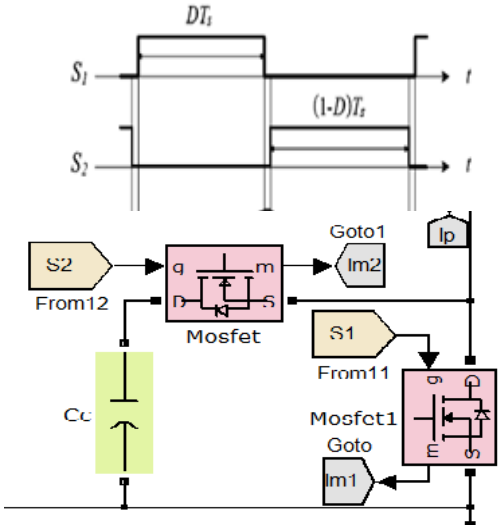


Fig. 2. Active clamp circuitry.

IV. CENTRE TAP TRANSFORMER

A tapped transformer T is used to limit the dc-link capacitor voltage Vd, where only one tap on the primary winding is required with one diode Db and boost inductor Lb with the turns ratio n of the transformer T defined as,

$$n = NS / NP, \text{ where } NP = NP1 + NP2 \quad \ldots(2)$$

And the dc-link voltage feedback value V_f is expressed as $$Vf = \frac{N_{P2}}{N_P} V_d \quad \ldots(3)$$

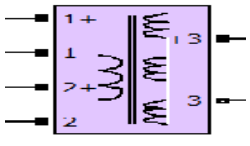


Fig. 3. Centre Tap Transformer.

While the transformer parameters are evaluated based on the data shown in Table

Table 2: Centre Tap Transformer Parameters.

Sin (Watts)	F (Hz)	Vp (Volts)	Vs (Volts)	Is (amps)
200	90K	230	60	3.5

V. VOLTAGE DOUBLER RECTIFIER

The resonant voltage-doubler rectifier consists of an inductor Ilk, capacitors Co1, Co2, and diodes Do1 and Do2. The inductors Lm and Llk are the magnetizing inductor and leakage inductor of the transformer "T". The currents iCo1 and iCo2 flow through the output resonant capacitors Co1 and Co2 and their sum of the currents iCo1 and iCo2 is the secondary resonant current is.

$$iCo1 = C_{o1} \frac{dVC_{o1}}{dt} = C_{o1} d\frac{(V_o - VC_{o2})}{dt}$$

$$= -C_{o2} \frac{dVC_{o2}}{dt} = iC_{o2} \quad \ldots(4)$$

The peak value of the currents iCo1 and iCo2 is half of the peak value of the secondary resonant current is. The output current io is half of the addition of the output diode currents iDo1 and iDo2 as

$$i_o = \frac{1}{2}(i_{Do1} + i_{Do2}) \quad \ldots(5)$$

The resonant process in the resonant voltage-doubler rectifier provides ZCS operation of the output diodes Do1 and Do2. Therefore, the power efficiency can be improved by reducing the reverse-recovery losses of the output diodes.

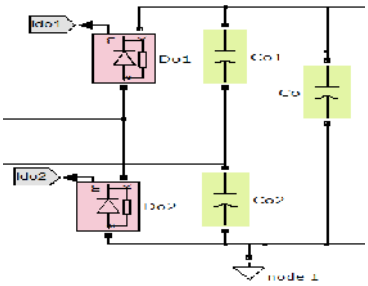


Fig. 4. Voltage doubler rectifier schematic.

VI. OPERATION PRINCIPLE

The converter topology under study has two operation regions. The line input voltage vi is given by $\sqrt{2}$Vi sin ωt, where Vi is the rms value and ω (= 2πf) is the angular line frequency. |vi | is rectified line input voltage.

When |vi | is higher than Vf, the converter works in region I. The output power Po is provided by the ac line.

When |vi | is lower than Vf, the converter operates in region II. The boost inductor current iLb does not flow since the diode Db is reverse biased. The boost inductor current iLb is assumed to be discontinuous. Figure 3 shows the equivalent circuit of the proposed converter in region I. Fig. .4 and 5 show the topological stages and key waveforms in region I. Here, D is the duty ratio of S1. The conduction times of the switches S1 and S2 are DTs and (1−D) Ts. The capacitors Cc, Cd, Co1, Co2, and Co are large enough so that the voltages Vc, Vd, VCo1, VCo2, and Vo are assumed to be constant. Moreover, |vi | is considered constant during one switching period Ts (= 1/fs), where fs is the switching frequency. Before t = t0, the voltage VS1 across S1 is zero, and the primary current ip is negative. Only the operation principle of region I will be described in this section. The operation principle of region II will not be described here. The operation principle of region II can be inferred without considering the boost inductor current iLb in the operation principle of region I.

The secondary resonant current is flowing through Do1 can be expressed as

$$i_s(t) = i_{D_{o1}}(t) = \frac{nV_d - V_{C_{o1}}}{\sqrt{L_{lk}/2C_{or}}} \sin\omega_r(t - t_0) \quad ...(6)$$

$$= i_{s\,peak} \sin\omega_r(t - t_0)$$

where the angular resonant frequency ω_r is given by:

$$\omega_r = 2\pi f_r = \frac{1}{2\sqrt{2L_{lk}C_{or}}} \quad ...(7)$$

Here, Llk is the leakage inductor of T, and Cor is the output resonant capacitor as Cor = Co1 = Co2 . Due to the magnetic coupling between NP1 and NP2 , the currents iNP1 and iNP2

$$i_{Lb}(t) = \frac{|v_i| - V_f}{L_b}(t - t_0) \quad ...(8)$$

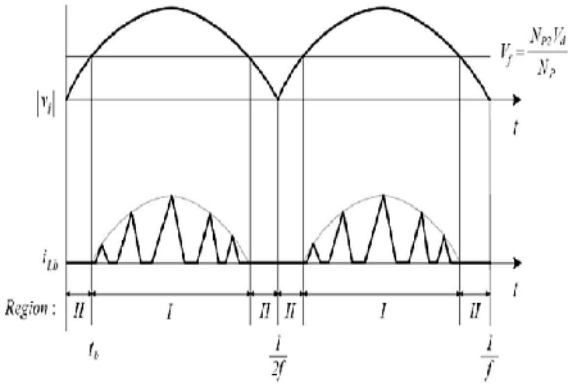


Fig. 5. Operation region of Converter.

$$i_{NP1}(t) = -\frac{N_{P2}}{N_P} i_{Lb}(t) + \frac{N_s}{N_P} i_s(t) \quad ...(9)$$

$$i_{NP2}(t) = \frac{N_{P1}}{N_P} i_{Lb}(t) + \frac{N_s}{N_P} i_s(t) \quad ...(10)$$

Then, the primary current ip is expressed as

$$i_p(t) = i_{Lm}(t) + \frac{V_d}{L_m}(t - t_0) + i_{NP2}(t)$$

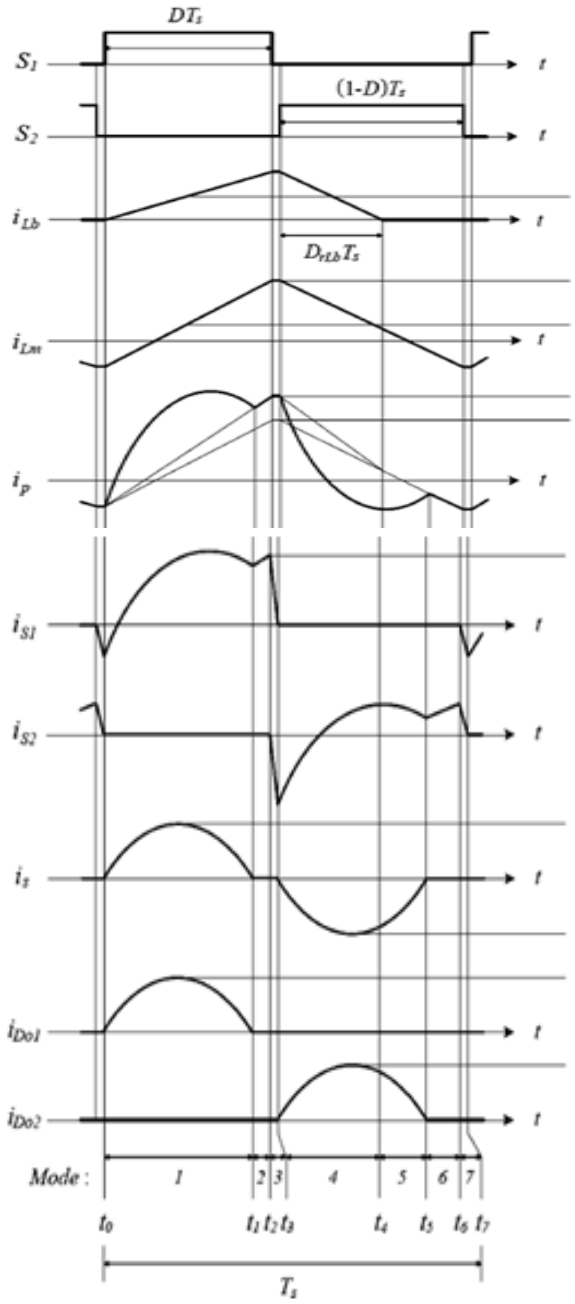


Fig. 6. Key waveforms of the proposed converter.

VII. ZVS BOOOST CONVERTER MODEL

The complete schematic of ZVS single stage boost type Active clamp is below in Figure 7.

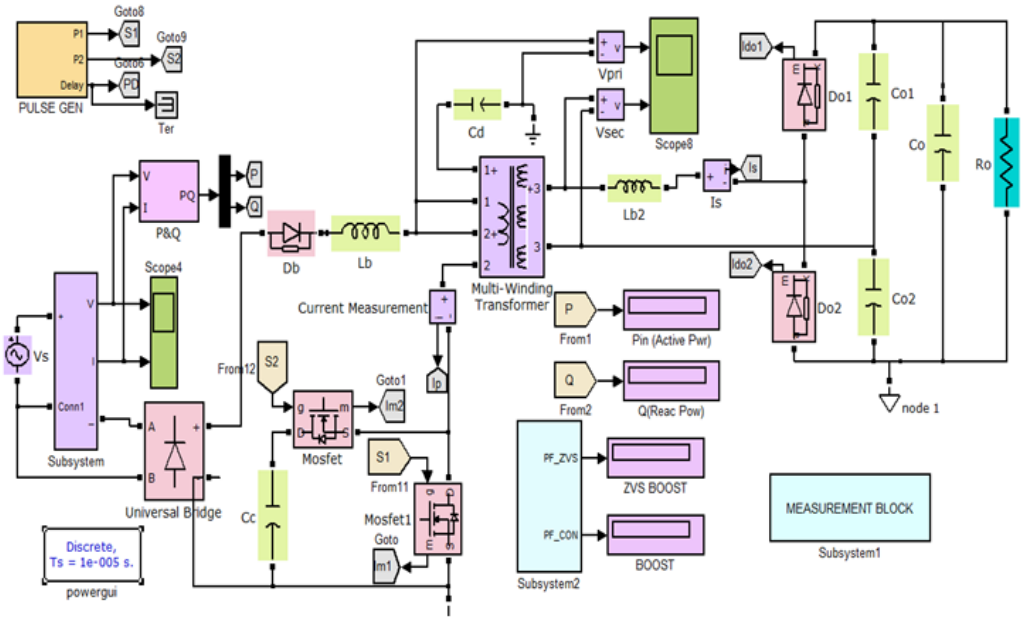
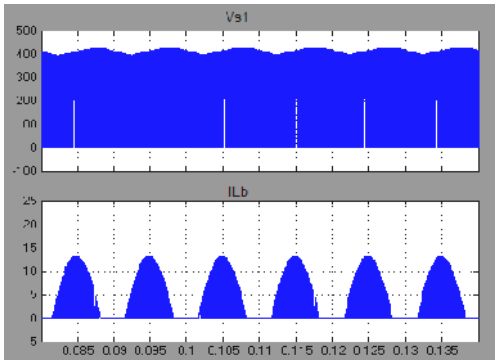


Fig. 7: Simulink model Developed for proposed converter.

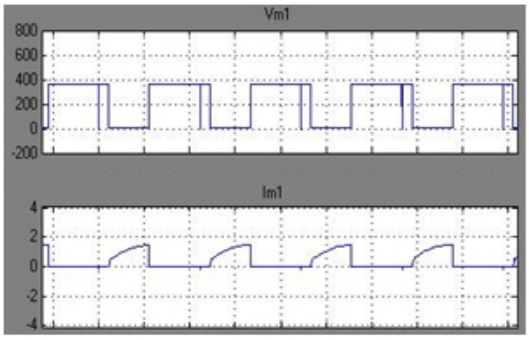
VIII. SIMULATION RESULTS

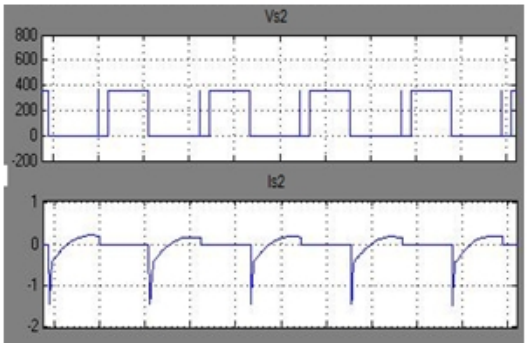
The simulation model prepared in the previous unit for a single stage zero voltage switching boost type active clamp circuitry was simulated using simulink®. The results obtained are validated with reference to the selected reference Choi et al [11] and are presented in the current section along with a discussion and analysis for the obtained waveforms.

The Converter model developed is simulated for an input voltage of 230 Vrms. The simulation result waveforms obtained are summarized.

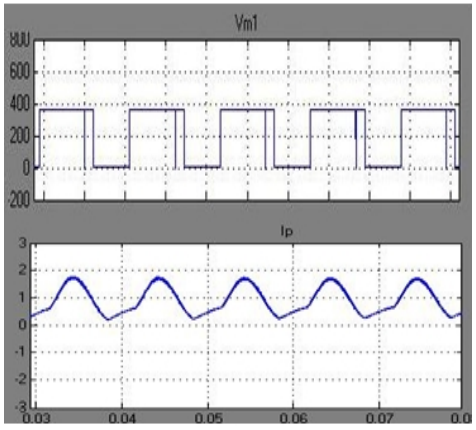


(a)

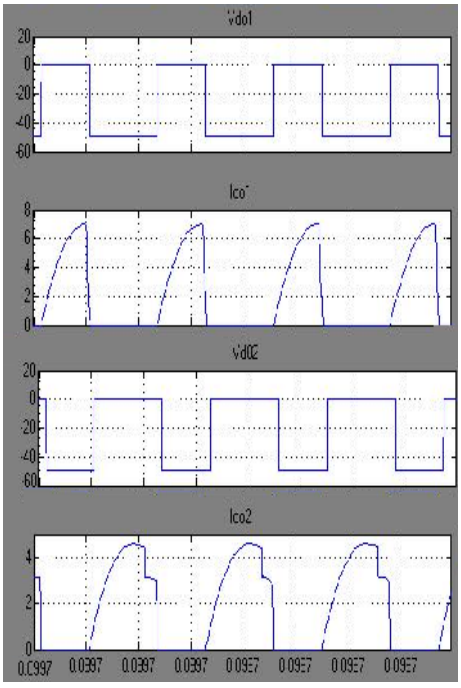




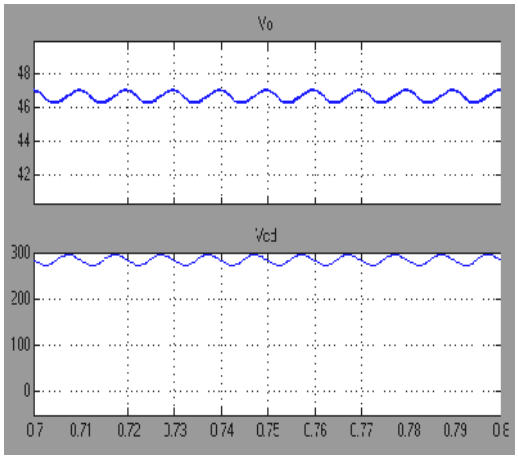
(b)



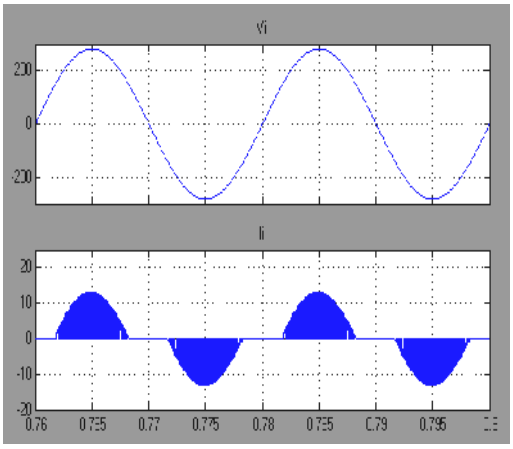
(c)



(d)



(e)



(f)

Fig. 8. Simulation Results obtained (a) Active clamp Switch Voltage and Boost Inductor Current (b) Active clamp voltage and current switch S1 and S2 (c) Switch Voltage and Transformer Primary Current (d) Voltage Doubler rectifier Voltage and current Diode Do1 and Do2 (e) Output voltage DC Link Capacitor Voltage (f) Input Voltage & Current.

IX. DISCUSION

MATLAB Simulink power system block set tool box has been used to estimate steady state performance of single stage zero voltage switching boost converter (ZVS) with active clamp circuitry, the Converter model is simulated for an input voltage of 230Vrms. The proposed converter has the following parameter as line voltage Vi=230Vrms output voltage 48V switching frequency fs=90kHz, boost inductor Lb=70µH, magnetizing inductor Lm=260µF, the DC Link capacitor Cd=220µF with a rated voltage 450 was used leakage inductor Llk 0.25µH clamp capacitor 2.2µF with rated voltage 630V, , the output capacitor Co = 680 µF with a rated voltage of 100 V was used since the output voltage ripple at twice the line frequency of the single-stage converter is poor, output resonant capacitor Cor=3.3µF with rated voltage 100V, switch output capacitor Cs=1.2µF. The Power factor obtained is much closer to unity as compared to a conventional AC-DC converter.

Fig.7 shows the dc-link voltage trajectory from no load to full load at 265-Vrms input voltage. The measured maximum dc-link voltage is 395 V. Therefore, the 450-V-rated bulk capacitor can be used in the proposed single-stage ac–dc converter.

Fig. 8(b) shows the simulation waveforms of the switches S1 and S2 at the line voltage of 230Vrms input for the rated load. As observed in the waveforms, the switch current changes after the switch voltages VS1 and VS2 become zero. It is shown that ZVS of the power switches is achieved. It can be also seen that there are no voltage spikes across the power switches.

Fig. 8(c) shows the waveforms of VS1 and ip at the line peak of 230Vrms input voltage for 160-W output power. It can be seen that the secondary resonant current is reflected to the primary side.

Fig. 8(d) shows the waveforms of the output diode Do1 and Do2 at the input line peak of 230Vrms for the rated load. Each output diode current becomes zero before each output diode is turned off. The output diodes are turned off naturally without any reverse-recovery process.

Fig. 8(e) shows the output voltage Vo and the dc-link capacitor voltage Vcd at 230-Vrms input voltage for the rated load. It can be seen that there is the voltage ripple across the dc-link capacitor. Meanwhile, the output voltage is tightly regulated for the rated load.

Fig. 8(f) displays measured input voltage and current waveforms for 160-W output power. Measured power factor is 0.989 with 92.4% efficiency at 230-Vrms input voltage.

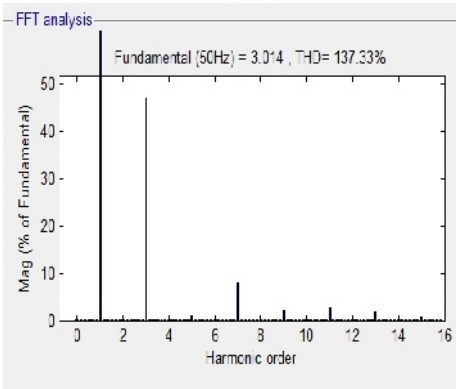


Fig. 9. FFT Analysis of Supply Current.

Fig. 9. **S**hows the measured line current harmonics. The line current harmonics were measured at 100- and 230-Vrms line input voltages. A comparison of proposed converter with that of conventional flyback converter is performed based on the simulation results obtained and the power efficiency of the conventional flyback converter is 89.3% at 90-Vrms input voltage. The maximum efficiency of the conventional flyback converter is 90.8% at 180-Vrms input voltage for 160-W output power. In the case of single-stage PFC flyback topology in [14], the power switch and the output diode operate under hard-switching condition. Also, the voltage stresses of the switching devices of the converter in [14] are higher than the voltage stresses of the switching devices of the proposed converter. Therefore, the switching power losses increase as the output power increases. The proposed converter improves the power efficiency by 2%, which gives approximately 20% reduction of the power loss compared to the converter in [14], by achieving soft-switching operation of the switching devices and reducing their voltage ratings.

X. CONCLUSION

A novel implementation of the PFC boost converter with an active clamp that can achieve soft-switching of all simulation A tapped transformer using a simple dc-link voltage feedback scheme was applied to the proposed converter for a practical design. At the secondary side, a resonant voltage-doubler rectifier helps the output diodes to achieve ZCS operation during their turnoff. Reverse-recovery-related losses in the boost diode are greatly reduced. The dc-link capacitor voltage is reduced, providing reduced voltage stresses of switching devices. Simulation results based on a 160W (48V/3.2 A) prototype have evaluated the performance of the proposed converter. The measured input current harmonics comply with the IEC 1000-3-2

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