



A Review of ALU Design Based on Fixed and Floating Point

Khushboo Dandotiya and Shraddha Shrivastava***

**PG Student, Department of Electronics and Communication Engineering,
LNCT Bhopal, (Madhya Pradesh), India*

***Assistant Professor, Department of Electronics and Communication Engineering,
LNCT Bhopal, (Madhya Pradesh), India*

(Corresponding author: Khushboo Dandotiya, dkhushi.789@gmail.com)

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ABSTRACT: In this present the review of ALU design technique based on different data processing technique. the design of ALU is major issue in current VLSI technology. The design of ALU is different segment of bit such as 8bit, 16bit, 32bit and many more design process of CPU. The efficiency of CPU processing data depends on the processing of ALU. The arithmetic logic unit (ALU) is the core of a CPU in a computer. The adder cell is the elementary unit of an ALU. The constraints the adder has to satisfy are area, power and speed requirements. Some of the conventional types of adders are ripple-carry adder, carry-look ahead adder, carry-skip adder and Manchester carry chain adder [7]. The delay in an adder is dominated by the carry chain. Carry chain analysis must consider transistor and wiring delays.

Keywords: ALU, CPU, Fixed point floating point.

I. INTRODUCTION

Arithmetic and Logic Unit (ALU) works as a data processing unit which is an important part in the central process unit (CPU) of any computer architecture. ALU is a multi-functional circuit that performs one of a few possible functions on two operands and which depends on the control inputs [6]. ALU needs to continually perform during the life-time of any computational devices such as a computer or a hand held device such as hand phone. Thus, reversible logic can be implemented in designing ALU to reduce the power dissipation and propagation delay in the circuits [1]. An arithmetic logic unit is a multi-functional circuit that conditionally performs one of several possible functions on two operands A and B depending on control inputs. It is nevertheless the main performer of any computing device. The ALU needs to continually perform during the life-time of any computational device such as a computer or a hand held device like PDA (Personal Digital Assistant) etc., Thus heat dissipation becomes a major issue in designing the ALU. Thus reversible logic can be aptly employed in designing the arithmetic logic unit. Also the ALU has to be resistant to the faults that may creep during the operation. Therefore it becomes more suitable that parity preserving reversible logic gates is used to design the ALU [3].

Reversible computing is a promising method in low power dissipating circuit design for current technologies such as low power Complementary Metal

Oxide Semiconductor (CMOS) design, cryptography, optical information processing, quantum computing and nanotechnology [4]. Reversible logic can be defined as thermodynamics of information processing. Hence, it is used to reduce the power dissipation by preventing the loss on information. is the block diagram of proposed reversible ALU designs. It has two main logic circuit design, namely, control unit and reversible full adder and the proposed design has five constants signals (e.g: Cinput1, Cinput2, Cinput3, Cinput4 and Cinput5) with a provision for realizing the eight arithmetic operations and four logic operations. Modern computers use conventions for representing non integer numbers, the most widespread of which is the IEEE 754 Standard for Floating-Point calculations. This standard defines binary representation for floating-point numbers of varying precision, giving specific examples of the binary 32 (or single precision) format, binary64 (or double precision) format and it defines operations on floating-point numbers.

The basic component of the arithmetic circuit of the ALU is the parallel adder. This is the basic structure, though high speed adders such as Carry Skip Adder, Look Ahead Carry Adder, Carry Save Adder etc., can be used instead of the parallel adder. The parallel adder (also called Ripple Carry Adder) is constructed with a number of full adders connected in cascade. By controlling the data inputs to the parallel adder, it is possible to obtain different types of arithmetic operations.

The rest of paper discuss as in section 2 discuss the Related Work. In section 3 discuss the parity preserving reversible gates and circuits. In section 4 discuss problem statement. Finally discuss conclusion & future work in section 5.

II. RELATED WORK

In this section we discuss the literature survey entitled with their author name and given references number respectively.

Lenin *et al.* [1] discussed designs, eight arithmetic and four logical operations are performed. In the discussed design, Peres Full Adder Gate (PFAG) is used in reversible ALU design and HNG gate is used as an adder logic circuit in the discussed ALU design. Both discussed designs are analyzed and compared in terms of number of gates count, garbage output, quantum cost and propagation delay. The simulation results show that the discussed reversible ALU design outperforms the discussed reversible ALU design and conventional ALU design. In this implement, the reversible ALU design is discussed with two unique design paradigms.

According to Mohd Zainolarifin *et al.* [2], heat sink is a component designed to minimize the temperature of the electronic component by dissipating the heat into it surrounding air. This implement proposes a new dimension of radial plate fin heat sink. The objective is to find the optimal design that could maximize the heat dissipation and minimize the size of heat sink on central processing unit electronic package. Based on the heat sink application reviews, thickness and the length of fins are considered for optimization. Model development of heat sink and multi objective using particle swarm optimization are explored for searching the optimal dimensions for radial plate fin heat sink design. Results and comparison of heat sink model and optimum values of the fitness functions for the radial heat sink are presented which show an increment of heat dissipation and reduction area.

De Peng Kong, *et al.* [3] describe modern warfare becomes more demanding on performance of the missile-borne computer: such as complexity of data process, real-time request, etc. Moreover, the computer application environment provides a strict restriction on system size and power dissipation. So a new design of digital processing platform with higher operation speed, greater capacity and lower power consumption is necessary to realize these. A design approach of an integrated guidance and control of missile-borne embedded computer system is discussed in this implement, which utilizes a multi-core DSP as the central data processing unit and a FPGA as the co-processing unit. Rakshith Saligram, *et al.* [4] researchers like Landauer and Bennett have shown that

every bit of information lost will generate $kT \log 2$ joules of energy, whereas the energy dissipation would not occur, if a computation is carried out in a reversible way. k is Boltzmann's constant and T is absolute temperature at which computation is performed. Thus reversible circuits will be the most important one of the solutions of heat dissipation in future circuit design. Reversible computing is motivated by the Von Neumann Landauer (VNL) principle.

Kamaraj Arunachalam, *et al.* [5] discussed, Reversible logic is an emerging technique, which has the ability to reduce power dissipation. The reversible circuits do not lose information and can generate unique outputs from specified inputs and vice versa. There is no loss of bits during its computation, which results in reduction in power dissipation. In this implement, an 8-bit arithmetic and logic unit (ALU) using reversible logic circuits is discussed and designed in Verilog HDL.

Parisa Safari, *et al.* [6] in this implement they are going to propose and analyze a basic model of fault tolerant reversible ALU and show that the realization of an efficient fault tolerant reversible ALU is possible with both minimum constant inputs and garbage outputs. The discussed fault tolerant reversible ALU is a versatile approach to the implementation of quantum computing with having both remarkable low power consumption and nano scaling. They have shown that a fault tolerant reversible basic arithmetic logic unit and a fault tolerant reversible 4×1 multiplexer as a block controller is possible. To do this they have used a parity preserving reversible gates for circuit design.

Suman Yadav and Manish Saxena *et al.* [7] described, in modern VLSI system power dissipation is very high due to rapid switching of internal signals. The complexity of VLSI circuits increases with each year due to packing more and more logic elements into smaller volumes. Hence power dissipation has become the main area of concern in VLSI design. In this implement, the design reversible ALU based on different types of reversible gate used with minimal delay, and may be configured to produce a variety of logical calculations.

Rangaraju *et al.* [8] discussed, Reversible computing is a promising alternative to these technologies, with applications in ultra-low power, nano computing, quantum computing, low power CMOS design, optical information processing, bioinformatics etc.

In reversible logic the power dissipation can be minimized or even eliminated. In this implement, the 4×4 reversible multiplier circuits is discussed with the design of new reversible gate called RAM gate. The discussed multiplier circuit is efficient compared to the existing designs in terms of gate counts, garbage outputs, constant inputs and quantum cost.

III. PARITY PRESERVING REVERSIBLE GATES AND CIRCUITS

A gate, a circuit or a function is reversible if and only if there is a one-to-one mapping between its input and output. Therefore, a reversible gate has an equal number of inputs and outputs. There is a number of commonly used reversible logic gate such as Feynman Gate, FG, Toffoli Gate, TG and Peres Gate, PG. Between reversible logic gates, those with their input parity being the same as their output parity are called "parity preserving reversible gates (circuits)" [7]. Most of arithmetic and other processing functions do not preserve the parity of the data. Parity checking is one of the most widely used methods for error detection in digital logic systems. Therefore it is important to construct parity preserving reversible gates and circuits. There are some problems using standard methods of error detection in reversible circuits, since fan-out is not allowed, and it may increase the number of gates being used along with the number of garbage outputs being produced. Given that reversible logic gates have the equal number of inputs and outputs, a sufficient requirement for parity preservation of a reversible circuit is that each gate to have a parity-preserving characteristics. Thus, a sufficient condition for having a parity preserving reversible logic gates is the implementation of the reversible circuit with each gate being parity preserving.

IV. PROBLEM STATEMENT

The design of digital circuit is always being challenging task for the processing of task and complex size. The designing of ALU give two types of fashion structure. On is tree and other is chain system. The utility of chain design system is very high. The design of ALU always compromised with high instruction cycle information transformation and emission of heat. The reducing the heating and number of instruction cycle always a challenging job. Some problem and issue discuss here in terms of ALU design.

- Implementation of a high performance arithmetic hardware with minimum possible clock cycles capable of computing square, square root and inverse in addition to basic arithmetic operations.

- Implementation of a fast data rate cache.

- Investigation of testing method to eliminate the need for additional hardware for testability while ensuring high fault coverage.

V. CONCLUSION AND FUTURE WORK

In this paper focus on Design of ALU was undertaken in the context of high performance and testability.

Architectures with high degree of parallelism were explored for design of high speed arithmetic unit. For simplicity, functional units were designed with 8-bit capability. Due to architectural parallelism, increase in operand size would only require replication of hardware parallel to existing circuitry. The ALU has standalone hardware for performing basic integer arithmetic operations and is capable of computing square, square root and inverse as well. A logic unit performing 8-bit logic operations was built using logic cells available in the IC cell library and was found to have a high operating frequency close to 1GHz. The multiplier is the most critical functional unit in the ALU. Popular techniques for improving the speed of a multiplier include reduction of the number of partial product rows, fast reduction of partial product rows and final summation of result using a fast adder.

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