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A comparative performance analysis of various CMOS design techniques for XOR and XNOR circuits

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ABSTRACT : In this paper, we review various design techniques for XOR-XNOR circuits as these circuits are basic building blocks of many arithmetic circuits. The XOR and XNOR circuits can be implemented in different architectures by using different circuit designs. This paper evaluates and compares the performance of various design techniques of XOR-XNOR circuits. The performance of the XOR-XNOR circuits based on TSMC 0.18µm process models at the supply voltage 1.8V is evaluated by the comparison of the simulation results obtained from HSPICE. The XOR and XNOR circuits with feedback transistors design are suitable for arithmetic circuits and other VLSI applications with very low power consumption and a very high speed performance.

Keywords : Exclusive-OR, Exclusive-NOR, High speed, Low power, Pass-Transistor Logic, Transmission Gate

I. INTRODUCTION

The semiconductor industry has witnessed an explosive growth of integration of sophisticated multimedia-based applications into mobile electronics gadgetry since the last decade. As the CMOS process technology shrinks, it has driven the VLSI industry towards very high integration density and system on chip designs and beyond few GHz operating frequencies, critical concerns have been arising to the severe increase in power consumption and the need to further reduce it. Moreover, the explosive growth driving the designers to strive for smaller silicon area, higher speeds, longer battery life, and more reliability. Power is one of the premium resources a designer tries to save when designing a system. The XOR-XNOR circuits are basic building blocks in various circuit especially-Arithmetic circuits (Full adder, and multipliers), Compressors, Comparators, Parity Checkers, Code converters, Error-detecting or Error-correcting codes, and Phase detector. The performance of the complex logic circuits is affected by the individual performance of the XOR-XNOR circuits that are included in them [1-7]. Therefore, careful design and analysis is required for XOR-XNOR circuits to obtained –full output voltage swing, lesser power consumption and delay in the critical path. Additionally, the design should have a lesser number of transistors to implement XOR-XNOR circuits and simultaneous generation of the two non-skewed outputs.

In this paper, performance of the PTL based XOR and XNOR circuits were evaluates and compares. Despite the saving in transistor count, the output voltage level of PTL based XOR-XNOR circuits is degraded at certain input combinations. The reduction in voltage swing, on one hand, is beneficial to power consumption. On the other hand, this may lead to slow switching in the case of cascaded operation. We propose and compare a PTL based new design techniques which produce the XOR-XNOR outputs simultaneously with full output voltage swing. The NMOS and PMOS transistors are added to the basic circuits to alleviate the threshold voltage loss problem commonly encountered in pass transistor logic design. To overcome the problem of skewed outputs basic XOR-XNOR designs are combined in one circuit.

The remainder of the paper is organized as follow. Section II gives the idea on previous work done on XOR and XNOR circuits in past two decades. Section III gives a short introduction to the various XOR and XNOR circuits design and compares them qualitatively. Results of quantitative comparisons based on simulations of different design techniques are shown in Section IV. Some conclusions are finally drawn in Section V.

II. PREVIOUS WORK

Exclusive–OR (XOR) and Exclusive-NOR (XNOR) circuits implement functions that are complementary. XOR and XNOR, denoted by $\oplus$ and $\odot$ respectively, are binary operations that perform the following Boolean Functions-

$$x \oplus y = x' y + x y'$$

$$x \odot y = x y + x' y'$$

In the past two decades, a number of circuit techniques have been reported with a view to improve the circuit performance of XOR-XNOR gates [1-14]. Albeit it is unusable to include every technique in the literature, in this section we have presented an overview of some significant techniques. A wide variety of XOR-XNOR implementations are available to serve different speed and density requirements.

Instead of cascading two 2-input XOR gates, a new design for 3-input XOR circuit is given in [4]. The reported circuit has the least number of transistors and no complementary input signals are needed. Especially, the power-delay product is also minimized.

A formal design procedure for realizing a minimal transistor CMOS pass network XOR cell is presented in [5]. This new cell can reliably operate within certain bounds when the power supply voltage is scaled down, as long as due consideration is given to the sizing of the MOS transistors during the initial design step. A low transistor count full adder cell using the new XOR cell is also presented in [5].

A PTL based 6-transitors XOR and XNOR circuits presented in [6] had full output voltage swing and better driving capability. To compare the performance of new circuit and test their driving capability, an adder circuit is built with the proposed XOR and XNOR circuits.

To compare the reported circuits in [7] comprehensively in a real application and test their driving capability, a circuit techniques for CMOS low-power high-performance multipliers circuit is design.

An XOR/XNOR function with low circuit complexity can be achieved with only 4 transistors in PTL [8]. Despite the saving in transistor count, the output voltage level is degraded at certain input combinations.

A new set of low power 4-transistor XOR and XNOR circuits called powerless (P-) XOR and Groundless (G-) XNOR respectively are proposed in [9-10]. The P-XOR and G-XNOR consumes less power than other design because it has no power supply (V_{DD}) or ground (V_{SS}) connection.

A new CMOS XOR circuit based on pass transistors is proposed in [11]. It uses only six transistors to produce both an XOR and the complementary XNOR function. The circuit has full voltage-swing and negligible static power dissipation. A drawback is that the transistors need to be ratioed due to a feedback structure. The main advantage of the new circuit was the reduction in device count.

A new 14 transistors full adder circuit was proposed in [12]. Although the device count is very low, the circuits have full voltage-swing in all nodes. This is achieved through the use of a 6 transistors CMOS XOR and XNOR function.

The Pass-Transistor Logic (PTL) is a better way to implement circuits designed for low power applications. The low power pass transistor logic and its design and analysis procedures were reported in [13-16]. The advantage of PTL is that only one PTL network (either NMOS or PMOS) is sufficient to perform the logic operation, which results in smaller number of transistors and smaller input loads, especially when NMOS network is used. Moreover, V_{DD}-to-GND paths, which may lead to short-circuit energy dissipation, are eliminated. These circuits have a non-full voltage swing at the output node and are characterized by its low power consumption. As the designs with fewer transistor count and lower power consumption are pursued, it becomes more and more difficult and even obsolete to keep full voltage swing operation. Note that in pass transistor logic, the output voltage swing may be degraded due to the threshold loss problem. That is, the output high (or low) voltage is deviated from the V_{DD} (or ground) by a multiple of threshold voltage. The reduction in voltage swing, on one hand, is beneficial to power consumption. On the other hand, this may lead to slow switching in the case of cascaded operation such as ripple carry adder. At low operation, the degraded output may even cause circuit malfunction.

In this paper, we review various design techniques for XOR-XNOR circuits based on static CMOS logic, PTL, DPL, Inverter and transmission gate etc. The XOR and XNOR circuits can be implemented in different architectures by using different circuit designs. Different types of circuit used to design XOR and XNOR circuits are discussed in Section III.

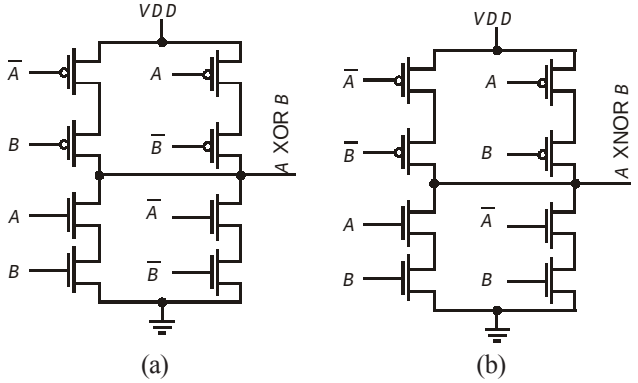
III. REVIEW OF VARIOUS XOR AND XNOR CIRCUIT DESIGN OF DIFFERENT CMOS LOGIC STYLES

A. Static CMOS XOR and XNOR circuit

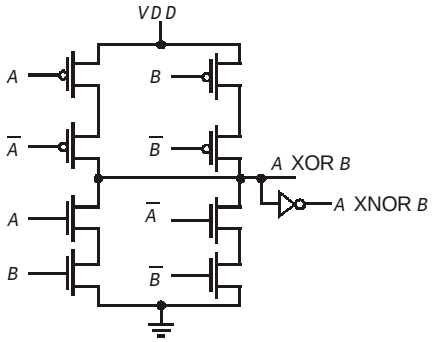
Complementary CMOS uses dual networks to implement a given function [1-3]. A first part consists solely of complementary pull-up PMOS network while a second part consists of pull-down NMOS networks. This technique is popular and produces results that are widely accepted one but it requires more numbers of CMOS transistors. Static CMOS XOR and XNOR gate is shown in Fig.1(a) and Fig.1(b). The circuit can operate with full output voltage swing.

$$Z = A \oplus B = (A + B) \,.\, (A' + B')$$
$$Z' = (A \oplus B)' = \{(A + B) \,.\, (A' + B')\}'$$
$$Z' = AB + A'B'$$
$$Z = (AB + A'B')' = A \oplus B$$

Alternative realization of static XOR and XNOR circuit using complementary CMOS transistors and above input-output relation is shown in Fig.1(c).



(a) (b)

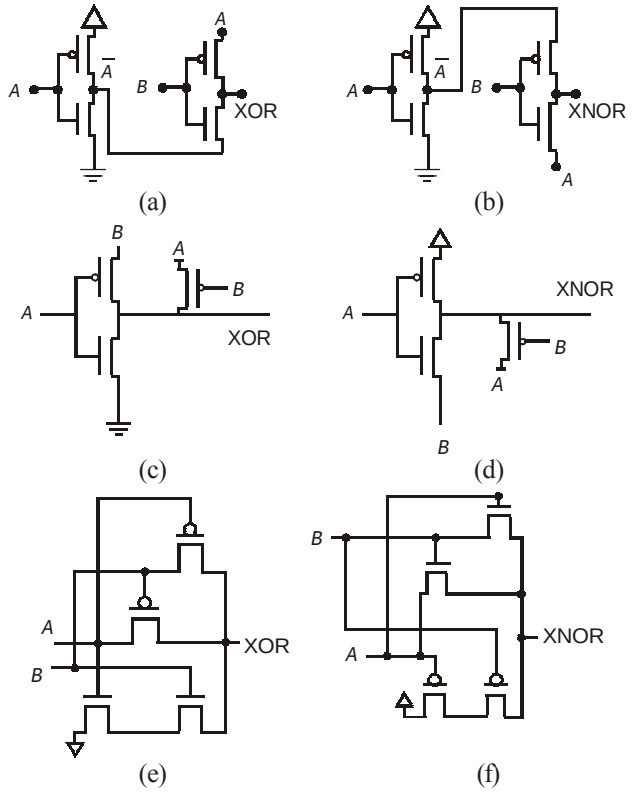


(c)

Fig.1. Static CMOS XOR circuit.

B. PTL based XOR and XNOR circuits

Another logic style, known as pass-transistor logic (PTL), is also commonly used. It differs from complementary CMOS in that the source side of the MOS transistor is connected to an input line instead of being connected to power lines. Another important difference is that only one PTL network (either NMOS or PMOS) is sufficient to perform the logic operation. Several XOR-XNOR circuits based on utilizing the high functionality of the pass transistor logic style are shown in Fig.2. Despite the saving in transistor count, the common problem encounter in all these circuits is threshold loss at the output node at certain input combinations. The reduction in output voltage swing, on one hand, is useful to power consumption. On the other hand, this may lead to slow switching in the case of cascaded operation such as ripple carry adder. At low V_{DD} operation, the degraded output may even cause circuit malfunction.



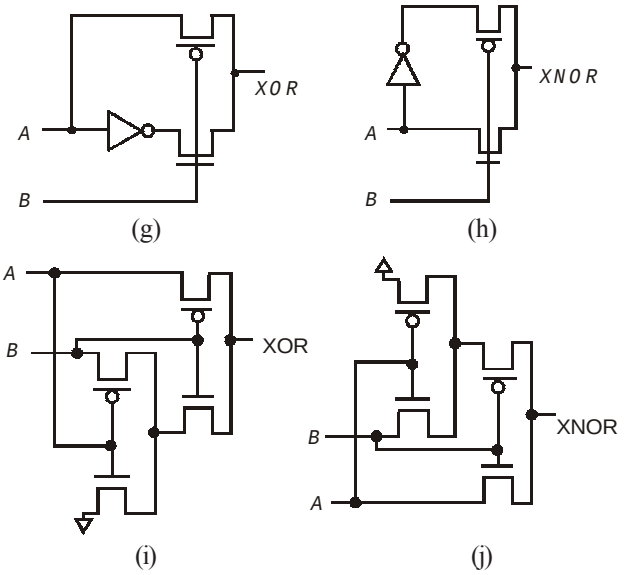


Fig.2. PTL Based XOR-XNOR circuits.

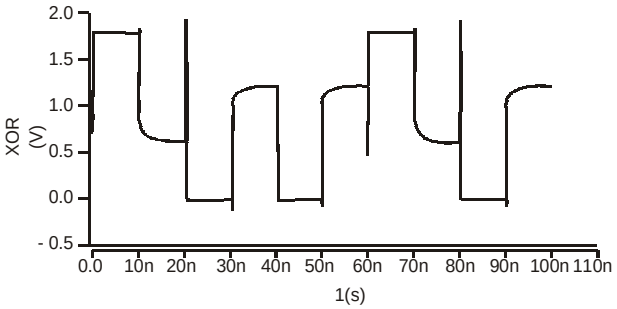


Fig.3(a). XOR output waveform for Fig.2(a).

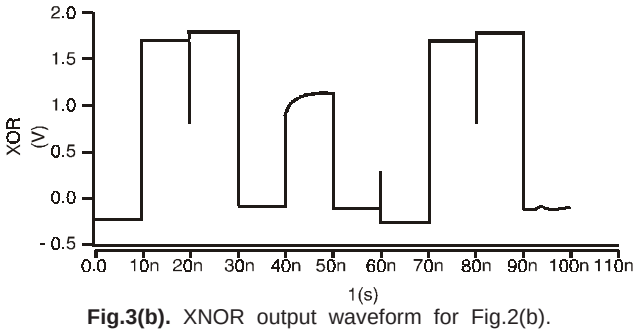


Fig.3(b). XNOR output waveform for Fig.2(b).

When the input *B* is at logic 1, the PMOS pass transistor is OFF and NMOS pass transistor is ON. Therefore the XOR output of the circuit in Fig.2(a) is the complement of input A and XNOR output in Fig.2(b) gets the same logic value as input A. When the input B is at logic 0, the XNOR output of the circuit in Fig.2(b) is the complement of input *A* and XOR output in Fig.2(a) gets the same logic value as input *A* for the reason that PMOS pass transistor is ON and NMOS pass transistor is OFF.

For XOR circuit in Fig.2(c), when the input *B* is at logic 1, the inverter circuit functions like a normal CMOS inverter. Therefore the output is the complement of input *A*. When the input *B* is at logic 0, the CMOS inverter output is at high impedance. However, the PMOS pass transistor is ON

and the output gets the same logic value as input *A*. The operation of the whole circuit is thus like a 2-input XOR circuit. However, it performs non full-swing operations for some input patterns causing their corresponding outputs to be degraded by $|V_{th}|$. For $A = 1$ and $B = 0$, voltage degradation due to threshold drop occurs across transistor and consequently the output is degraded with respect to the input. For XNOR circuit in Fig.2(d), when $A = 0$ and $B = 1$, voltage degradation due to threshold drop occurs across transistor and consequently the output is degraded with respect to the input.

The XOR and XNOR circuit respectively in Fig.2(e) and Fig.2(f) has degraded output voltage swing, limited driving capability and is characterized by low power consumption.

The circuits in Fig.2(g) and Fig.2(h) are provides good output levels and the driving capability of the circuits is also improved as it uses static CMOS inverter. The main limitation of the circuits is extra power consumption due to the presence of the static CMOS inverter.

A new set of low power 4-transistor XOR and XNOR circuits called powerless (P-) XOR and Groundless (G–) XNOR respectively are shown in Fig.2(i) and Fig.2(j). The XOR circuit in Fig.2(i) is similar to the XOR circuit in Fig.2(g). The only difference is that the V_{DD} connection of the static CMOS inverter is connected to the one of the two inputs signals. The P-XOR and G-XNOR consumes less power than other design because it has no power supply (V_{DD}) or ground (V_{SS}) connection. These circuits are unable to function properly at low supply voltage due to threshold loss at the output node and displayed poor delay characteristics.

C. DPL XOR and XNOR circuits

Double pass-transistor logic (DPL) uses complementary transistors to keep full swing operation and reduce the dc power consumption. This eliminates the need for restoration circuitry. One limitation of DPL is the large area used due to the presence of PMOS transistors. 10-transistors DPL (Double pass-transistor logic) XOR and XNOR circuits are shown in Fig.4 have been design to improve circuit performance at low supply voltages [17].

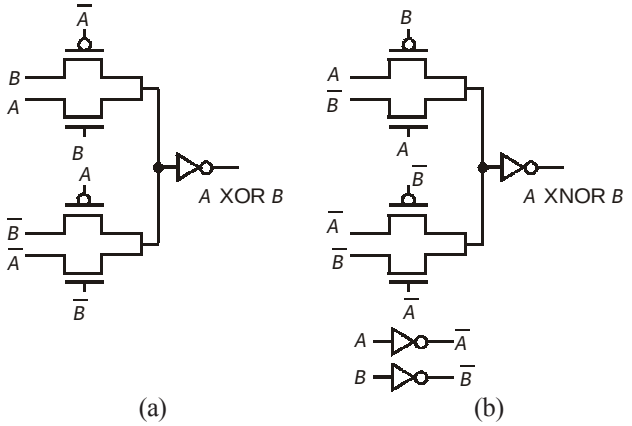


Fig.4. DPL XOR and XNOR circuit.

Because of the presence of both NMOS and PMOS devices, all nodes in DPL circuits have a full voltage swing and there is no static short-circuit current problem. The drawback of this circuit is the required complementary inputs.

D. Inverter based XOR and XNOR circuits

Inverter based XOR and XNOR circuits [17] are design by cascading three inverters as shown in Fig.5. The serious limitation of these circuits is non full voltage swing at the internal nodes of the circuit. However, they operate reliably at high supply voltage. The output value for the Fig.5 shown in Table 1, showing the signal levels at the output, are seen to be degraded in some cases at a low supply voltage of 1.8 V.

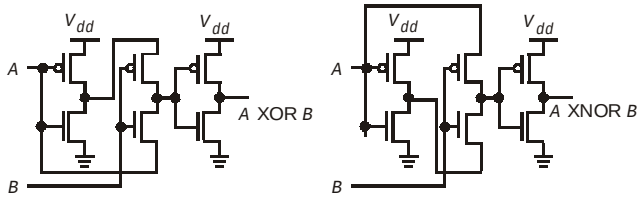


Fig.5. Inverter based XOR and XNOR circuits.

Table 1 : Input and output values for the Fig.5.

Inputs		Output	
A	**B**	**XNOR**	**XOR**
0	0	Bad 1	Good 0
0	1	Good 0	Good 1
1	0	Good 0	Good 1
1	1	Good 1	Good 0

E. Transmission gate based XOR and XNOR circuits

Transmission gate CMOS (TG) uses transmission gate logic to realize complex logic functions using a small number of complementary transistors. It solves the problem of low logic level swing by using PMOS as well as NMOS.

10-transistor circuits for XOR-XNOR function [18] based on transmission gates and inverters is shown in Fig.6. This circuit rectifies the flaws in the previous designs. The design is composed of two transmission gates and three static inverters. In this design, an inverter is employed to generate the complementary signal of XOR function as XOR and XNOR circuits implement functions that are complementary [19]. This circuit can operates at lower supply voltage and have a full output voltage swing for all input combinations. Also, the uses of static CMOS inverters enhance the driving capability at the cost of extra power consumption. This type of design has the disadvantage of delaying one of the XOR and XNOR outputs, giving rise to skewed signal arrival time to the successive modules. This will increase the chance of producing spurious switching and glitches in the output.

The limitation of the PTL based XOR, XNOR circuits comes from the fact that their internal nodes do not have a full voltage swing. Thus, the noise margins are reduced and the output stage looses part of its capability to drive larger loads. The result is the circuits do not operate reliably at a low supply voltage.

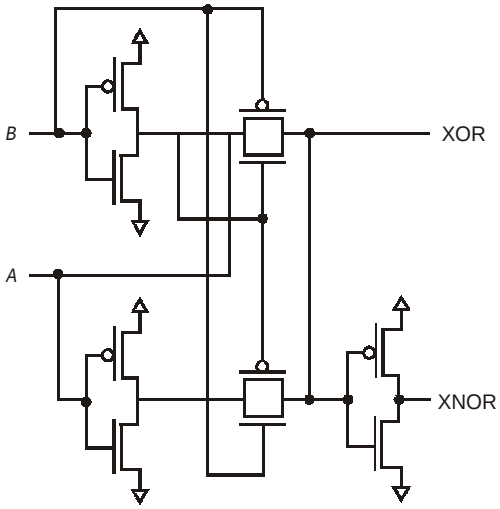


Fig.6. 10-transistor circuits for XOR-XNOR function.

To achieve a full-voltage swing transmission based XOR and XNOR circuits are design as shown in Fig.7. This circuit alleviate the problems of threshold voltage loss and provide a full voltage swing at the outputs as shown in Fig.7(c).

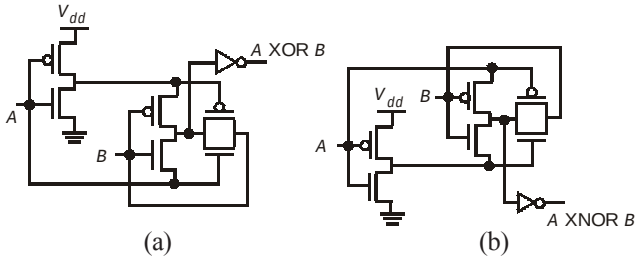


Fig.7. High performance transmission gate XOR, XNOR circuits.

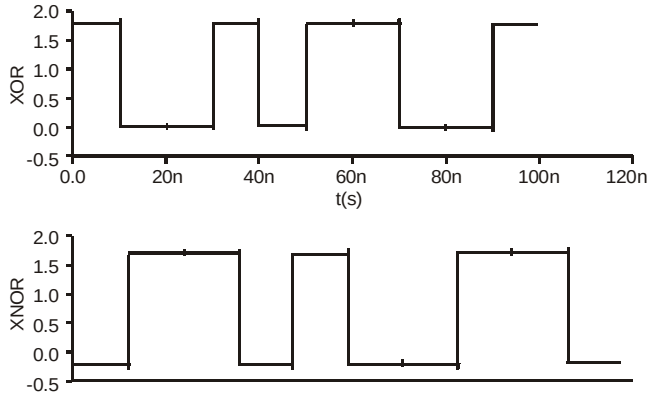


Fig.7(c). Output waveform for XOR and XNOR circuit in Fig.5(a) and Fig.5(b).

The 9-transistor circuits for XOR-XNOR function [20] is shown in Fig.8 alleviate the problems of threshold voltage loss and non-zero standby power dissipation. By cascading a standard inverter after the XOR circuit, a high performance XNOR, as shown in Fig. 8(a) will have a restored output. The same property is present in the XOR structure. The output value for the Fig.8 shown in Table 2, showing the signal levels at the output, are seen to be correct in all cases at a low supply voltage of 1.8 V. These circuits provide a full voltage swing (*i.e.*, 0V for logic 0 and 1.8V for logic 1).

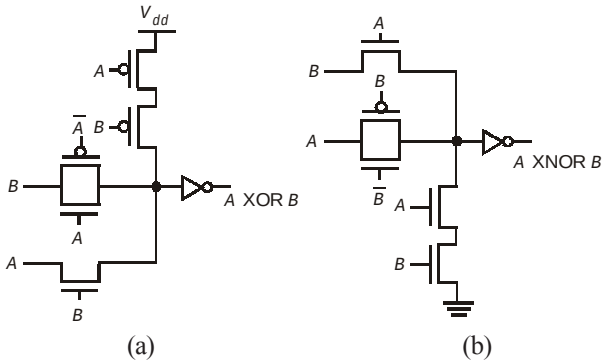


Fig.8. Transmission gate XOR, XNOR circuits.

Table 2 : Input and output values for XOR and XNOR circuits in Fig.8.

Inputs		Output	
A	**B**	**XNOR**	**XOR**
0	0	Good 1	Good 0
0	1	Good 0	Good 1
1	0	Good 0	Good 1
1	1	Good 1	Good 0

F. GDI XOR circuit

GDI (Gate diffusion input) is a low-power digital combinational circuit design technique is based on the use of a simple GDI cell as shown in Fig.9(a). The basic difference between GDI cell and standard CMOS inverter is as follow :

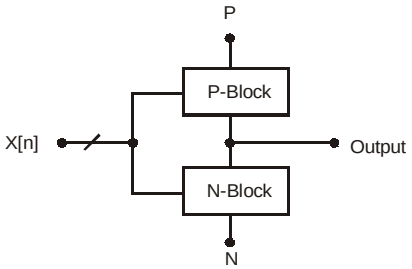


Fig.9(a). (n + 2) inputs GDI cell.

The GDI cell contains three inputs – G (common gate input of NMOS and PMOS transistor), *P* (input to the source/drain of PMOS), and *N* (input to the source/drain of NMOS).Bulks of both NMOS and PMOS are connected to *N* or *P* (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter.

This technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. 4-transistors XOR circuit using GDI cell [21] is shown in Fig.9(b).

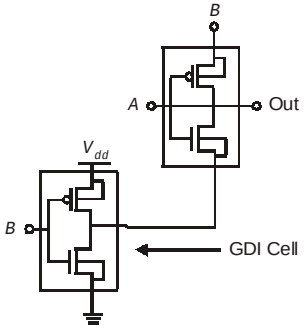


Fig.9(b). GDI XOR circuit.

G. XOR and XNOR circuits with feedback transistors

The combined XOR-XNOR cell is used to drive the selection lines of the multiplexer, control signal lines etc, the simultaneous generation of the two non-skewed outputs is highly desirable. To overcome the problem of the skewed outputs some designs that combine the implementation of both the XOR and XNOR functions in one circuit are discussed below. While to improve the output voltage swing the cross-coupled PMOS transistors and/or cross- coupled PMOS and NMOS transistors are connected between XOR and XNOR outputs.

The XOR and XNOR circuit reported in [22] is based on non-complementary input signals and has a better PDP and noise immunity. The NMOS and PMOS transistors are added to the basic circuits to alleviate the threshold voltage loss problem commonly encountered in pass transistor logic design. To overcome the problem of skewed outputs basic XOR-XNOR designs are combined in one circuit as shown in Fig.10(a). At very low voltages the power dissipation becomes negligible as compared to the reduction in delay and the power-delay product of this circuit is always better than its counterparts. The output is glitch free and is shown in Fig.10(b).

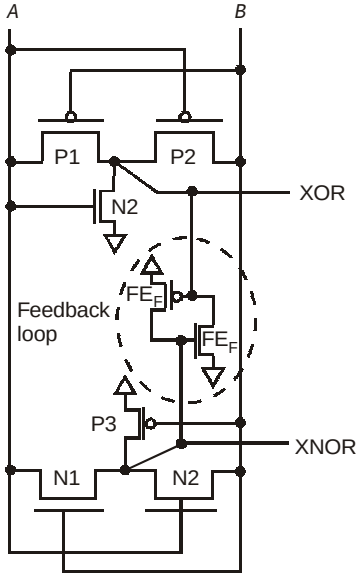


Fig.10(a). XOR–XNOR circuits.

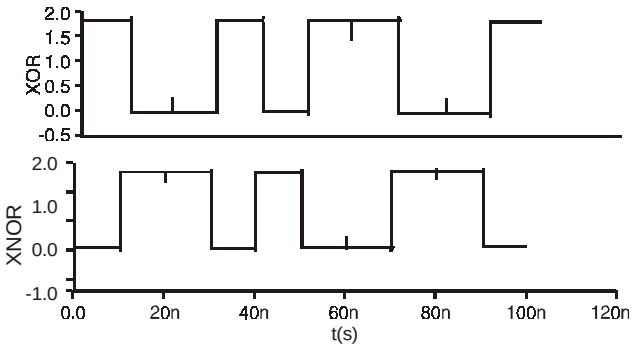


Fig.10(b). Output waveform for XOR-XNOR circuit in Fig.10(a) and Fig.10(b).

This circuit is based on complementary input signals. In this methodology, the number of transistors increases but the performance is greatly improved. Another highlight of this methodology is the use of feedback transistors [23-24].

The first circuit is shown in Fig.11(a). Two pull-up transistors *P*1 and *P*2 and two pull-down transistors *N*1 and *N*2 (Shown with the dotted circles) augment the basic skeleton (shown with the shaded area). The output value for the basic circuit is shown in Table 3 and output waveform of the XOR and XNOR circuit after application of methodology-I is shown in Fig.11(c). As it can be seen in the table, alternate output value is a bad or a weak logic. Specifically, input vector "10" produces "bad 1" for XOR function. This is rectified by the use of the two pull-up transistors *P*1 and *P*2 in the XOR network.

Table 3 : Input and output values for the basic circuit.

Inputs		Output	
A	**B**	**XNOR**	**XOR**
0	0	Good 1	Bad 0
0	1	Bad 0	Good 1
1	0	Good 0	Bad 1
1	1	Bad 1	Good 0

Similarly, for XNOR function, input vector "01" produces a "bad 0", and this can be rectified by the use of the two pull-down transistors *N*1 and *N*2 in the XNOR network. The remaining two bad outputs are corrected by using a feedback loop (shown in Fig. with the dotted square).

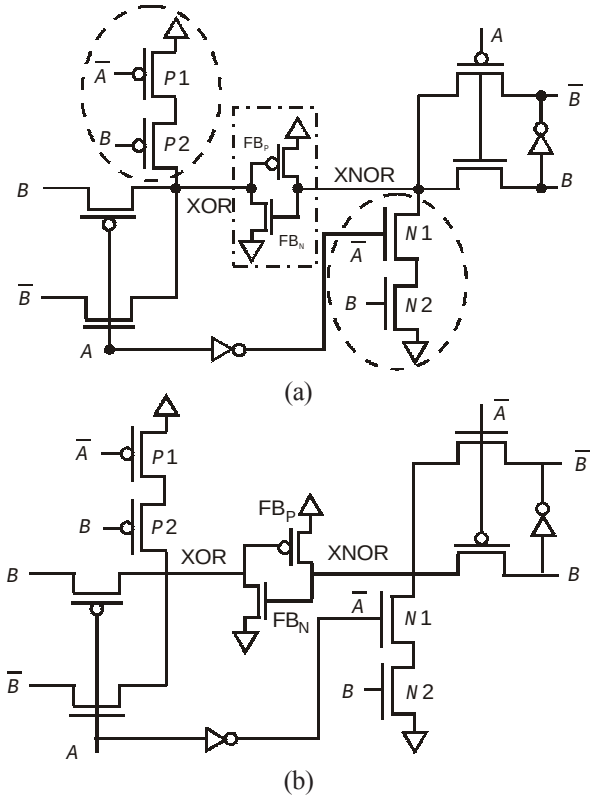


Fig.11. XOR –XNOR circuits.

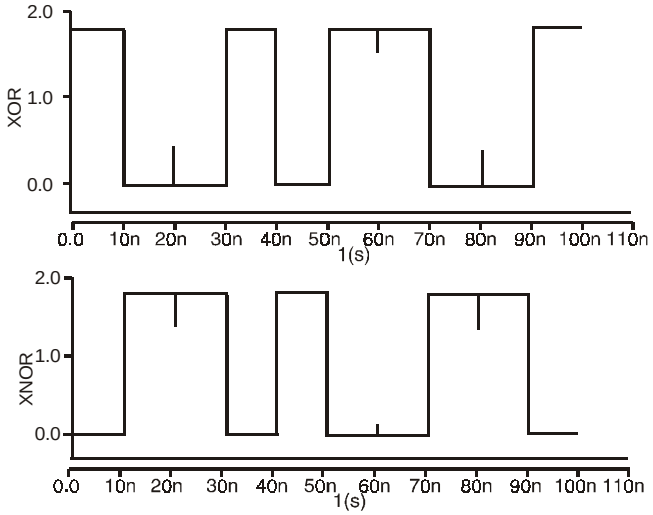


Fig.11(c). Output waveform for XOR and XNOR circuits in Fig.11(a) and Fig.11(b).

The reported circuit in [23-24] is consisting of complementary input signals and forward and backward feedback loops. The dual feedback network is used to rectify the degraded logic level problem i.e. forward feedback loop is used to improve the output voltage level for input combinations (00) and (11) while the backward feedback loop is used to enhance the output logic level of the circuit for input combinations (01) and (10). This feedback configuration enhances the circuit performance as well as fan out also. The reported dual feedback network is shown in Fig.12.

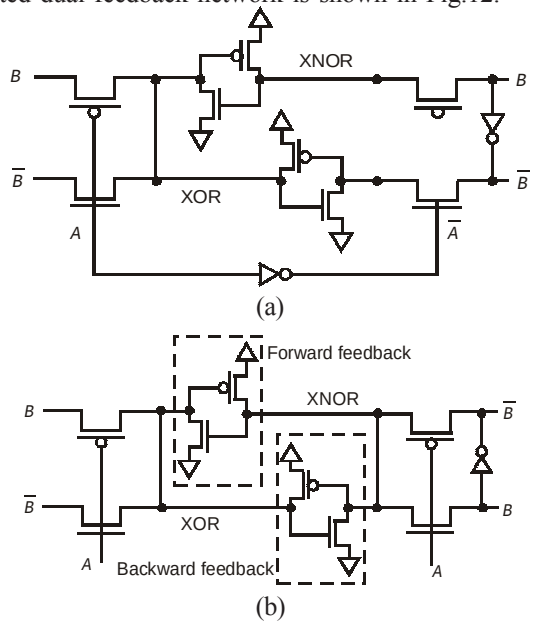


Fig.12. XOR –XNOR circuits.

Table 4 : Input and output values for XOR and XNOR circuits for Fig.12.

Inputs		Output	
A	**B**	**XNOR**	**XOR**
0	0	Good 1	Good 0
0	1	Good 0	Good 1
1	0	Good 0	Good 1
1	1	Good 1	Good 0

To overcome the problem of skewed outputs the basic 6-transistors XOR and XNOR circuit designs are combined in one circuit and the cross-coupled PMOS and NMOS transistors are connected between XOR and XNOR outputs [25] as shown in Fig.13. The circuit has a single connection to V_{DD} and a single connection to ground with no direct connection between them. The existence of V_{DD} and ground connections gives good driving capability to the circuit and the elimination of direct connections between them avoids the short circuit currents component.

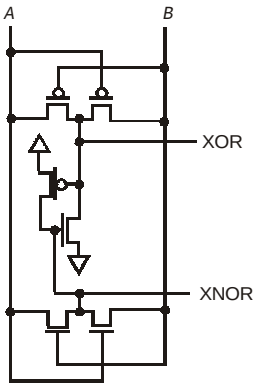


Fig.13. XOR-XNOR circuit.

A novel 8-transistors XOR–XNOR circuit that generates XOR and XNOR outputs simultaneously is shown in Fig.14. This circuit provides a full voltage swing (*i.e.,* 0V for logic 0 and 1.8V for logic 1) at low supply voltage. The reported XOR–XNOR circuit [26-27] is based on complementary pass-transistor logic using only one static inverter instead of two static inverters as in the regular CPL style XOR circuit. The first half of the circuit utilizes only NMOS pass transistors for the generation of the XOR and XNOR outputs. The cross-coupled PMOS transistors are connected between XOR and XNOR output to alleviate threshold problem for all possible input combinations and reduce short-circuit power dissipation. The circuit is inherently fast due to the high mobility NMOS transistors and the fast differential stage of cross-coupled PMOS transistors. Table 5 indicates the functioning of the XOR-XNOR circuit shown in Fig.14 more clearly.

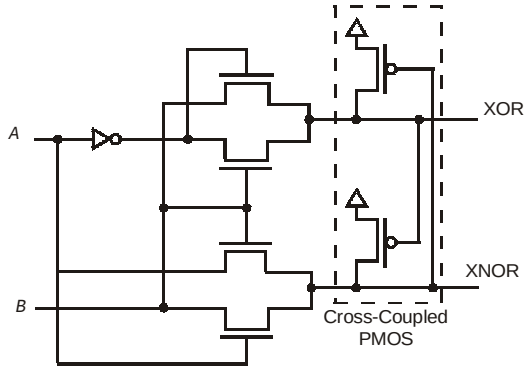


Fig.14. XOR-XNOR circuit.

Table 5 : Input and Output values for XOR and XNOR circuits for Fig.14.

Inputs		Output	
A	B	XNOR	XOR
0	0	Good 1	Good 0
0	1	Good 0	Good 1
1	0	Good 0	Good 1
1	1	Good 1	Good 0

The reported XOR-XNOR circuit in [28], as shown in Fig.15(a) has two complementary feedback transistors to restore the non full voltage swing. They restore the non full-swing output by either pulling it up through PMOS to the V_{DD} or down through NMOS to ground. This will increase the driving capability. In addition, since there is no direct path between the power supply and ground, short-circuit current has been reduced.

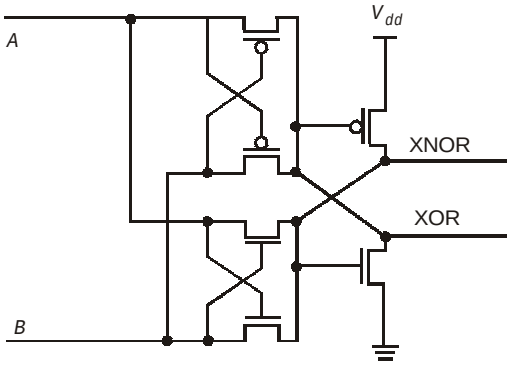


Fig.15(a). XOR-XNOR circuits.

Due to the unsatisfactory performance at low-supply voltage, we modified the circuit of Fig.15(a) to Fig.15(b). In this circuit the two series PMOS and NMOS transistors are added to solve the worst-case delay problem. This circuit has full output voltage swing for all possible input combinations as shown in Fig.15(c).

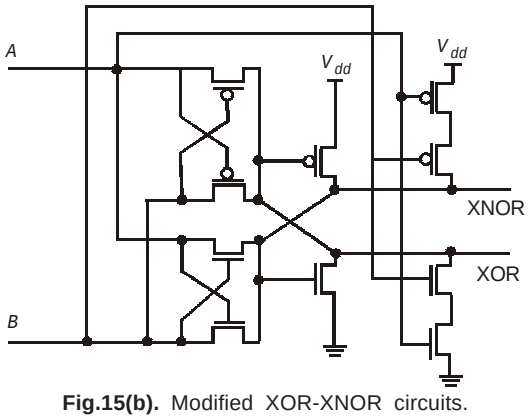
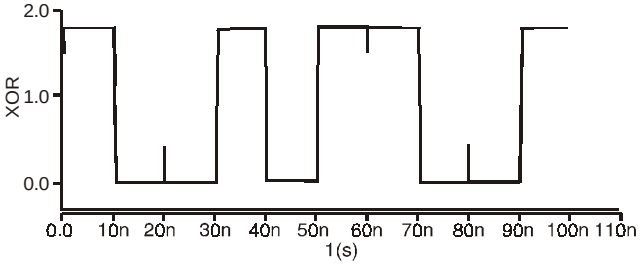


Fig.15(b). Modified XOR-XNOR circuits.



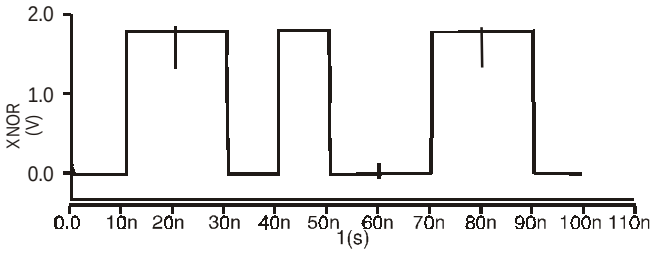


Fig.15(c). Output waveform for XOR and XNOR circuits shown in Fig.11(b).

IV. SIMULATION RESULTS AND COMPARISON

The transient and DC analysis of the circuits were performed on HSPICE at a supply voltage ranging 0.6V to 3.3V using TSMC 0.18µm CMOS process. TSMC 0.18µm SPICE transistor parameter for NMOS and PMOS transistors are given in appendix. A constant output load capacitance of 5.6fF is used for power and delay measurements. The simulation test bench used is shown in Fig.16. All possible input combinations at the gate inputs were simulated. The input waveforms used for the simulation of various XOR and XNOR designs are shown in Fig.17.

The comparative performance for all PTL based XOR and XNOR circuit designs at V_{DD} = 1.8V are respectively shown in Table 6 and Table 11.

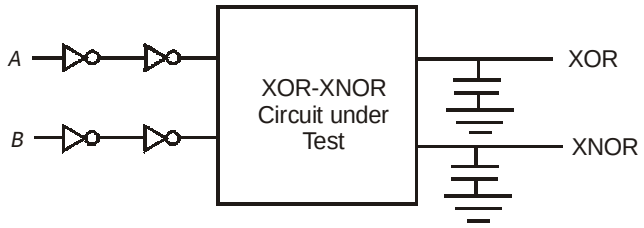


Fig.16. Simulation test bench.

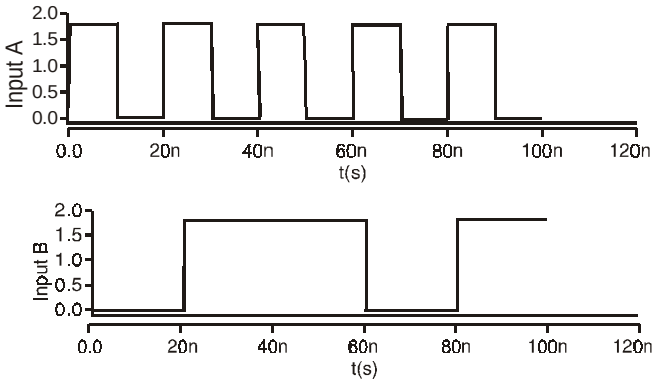


Fig.17. Input waveforms for the proposed techniques.

Table 6 : Comparative performance of transient analysis of Static CMOS XOR and XNOR circuits at V_{DD}= 1.8V.

	Fig.1(a)	Fig.1(b)	Fig.1(c)
# of transistors	12	12	14
Delay XOR (ns)	0.046	–	0.0595
Delay XNOR (ns)	-	0.086	0.088
Average Dynamic Power Consumption (X E-05W)	6.8389	6.4430	7.7644
PDP (fJ)	3.1458	5.5409	6.8326
EDP(ns*fJ)	0.1447	0.4765	0.6013

Table 7 : Comparative performance of transient analysis of PTL based XOR circuits at V_{DD}= 1.8V.

	Fig.2(a)	Fig.2(c)	Fig.2(e)	Fig.2(g)	Fig.2(i)
# of transistors	4	3	4	4	4
Delay XOR (ns)	0.0415	0.055	0.1325	0.22	0.231
Average Dynamic Power Consumption (X E-05 W)	6.3513	0.3638	2.97	1.122	2.5872
PDP (fJ)	2.6357	2.0009	3.9352	2.4684	5.9764
EDP(ns*fJ)	0.1094	0.11	0.5214	0.5430	1.3805

Table 8 : Comparative performance of transient analysis of PTL based XNOR circuits at V_{DD}= 1.8V.

	Fig.2(b)	Fig.2(d)	Fig.2(f)	Fig.2(h)	Fig.2(j)
# of transistors	4	3	4	4	4
Delay XNOR (ns)	0.037	0.0395	0.1055	0.44	0.422
Average Dynamic Power Consumption (X E-05W)	6.22	0.3408	2.9316	1.1338	3.3912
PDP (fJ)	0.2301	0.0134	0.3093	0.4988	1.4311
EDP(ns*fJ)	0.0085	0.0005	0.0326	0.2195	0.6039

Table 9 : Comparative performance of transient analysis of DPL and inverter based XOR and XNOR circuits at V_{DD}= 1.8V.

	Fig.4(a)	Fig.4(b)	Fig.5(a)	Fig.5(b)
# of transistors	10	10	6	6
Delay XOR (ns)	0.0715	-	0.0825	-
Delay XNOR (ns)	-	0.0825	-	0.085
Average Dynamic Power Consumption(X E-05W)	6.9402	6.9199	6.5126	43.727
PDP (fJ)	0.4962	0.5709	0.5373	3.7167
EDP(ns*fJ)	0.0355	0.0471	0.0443	0.3159

Table 10 : Comparative performance of transient analysis of transmission gate XOR-XNOR circuits at V_{DD}= 1.8V.

	Fig.6	Fig.7(a)	Fig.7(b)	Fig.8(a)	Fig.8(b)
# of transistors	10	8	8	9	9
Delay XOR (ns)	0.1695	0.0950	-	0.0813	-
Delay XNOR (ns)	0.193	-	0.0765	-	0.0761
Average Dynamic Power Consumption(X E-05W)	9.24	7.076	6.89	6.42	6.93
PDP (fJ)	1.7833	0.6722	0.5271	0.5219	0.5273
EDP(ns*fJ)	0.3442	0.0638	0.0403	0.0424	0.0401

Table 11 : Comparative performance of transient analysis of XOR-XNOR circuits with feedback transistors at V_{DD}= 1.8V

	Fig.10(a)	Fig.11(a)	Fig.11(b)	Fig.12(a)	Fig.12(b)	Fig.13	Fig.14	Fig.15(a)	Fig.15(b)
# of transistors	8	14	14	10	12	6	8	6	10
Delay XOR (ns)	0.1435	0.1570	0.0785	0.0995	0.0725	0.0965	0.0645	0.092	0.0815
Delay XNOR (ns)	0.1175	0.1585	0.1325	0.1155	0.1295	0.036	0.0575	0.0495	0.061
Average Dynamic Power Consumption (X E-05W)	8.11	13.43	9.78	16.47	20.13	9.11	18.58	5.97	7.21
PDP (fJ)	11.638	21.286	12.958	19.02	26.068	8.791	11.984	5.492	5.8761
EDP(ns*fJ)	1.670	3.373	1.717	2.197	3.3758	0.848	0.7729	0.5492	0.4789

V. CONCLUSION

In this paper, we have reviewed various design techniques for XOR-XNOR circuits. The mentioned design techniques are compared based on a delay, power consumption, and PDP, EDP. The performances of these techniques have been evaluated by HSPICE using a TSMC 0.18µm CMOS technology. These design techniques are suitable for arithmetic circuits and other VLSI applications with very low power consumption and a very high speed performance. Based on the simulation results, it has been culminated that in the PTL based XOR and XNOR design the output high (or low) voltage is deviated from the V_{DD} (or ground) by a multiple of threshold voltage. The XOR-XNOR circuits using transmission gate improve the threshold voltage loss problem while XOR and XNOR circuits with feedback transistors have good output signal levels, consume less power and have high speed compared to the previous designs at low supply voltage.

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