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Silicon carbide GTO thyristor for HVDC converter

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ABSTRACT : With the increase in use of power electronics in transmission and distribution applications there is a growing demand for cost effective and highly efficient converters. Most of the utility applications have power electronics integrated in the system to improve the efficiency and functionality of the existing system. The development of semiconductor devices is vital for the growth of power electronics system. Modern technologies like voltages source converter (VSC) based HVDC transmission has been made possible with the advent of power semiconductor devices like IGBT and GTO thyristor with their high power handling capability.

Various material limitations of silicon power semiconductor devices have led to the development of wide band gap semiconductors such as SiC, GaN and diamond. Silicon Carbide is the most advanced from research to manufacturing phase. This project presents the modeling and design of a loss model of 4H-SiC GTO thyristor device, and the effect of device benefits at system level are studied. The device loss model has been developed based on the device physics and device operation, and simulations have been conducted for various operating conditions. The thesis focuses on the study of a comparison between silicon and silicon carbide devices in terms of efficiency and system cost savings for HVDC transmission system.

Keywords : HVDC, Silicon Carbide, GTO, Thyristor, HVDC Transmission.

I. INTRODUCTION

The thyristor is the key component of a converter bridge, and improvements in thyristor ratings and characteristics highly influence the costs of the valves, and other equipment in a converter substation. GTO, a device with turn off capability in the thyristor family, is making a significant impact in power-electronic design. The turn-off capability feature has evolved new circuit concepts such as self-commutated, pulse-width modulated (PWM), voltage-driven and multi-step converters, and enables the circuits to operate at higher switching frequencies. These, in turn, reduce harmonic content and allow operation at leading power factors.

GTOs are attractive for dc power conversion into ac systems, which have little or no voltage support and hence are gaining wider attention in their application to HVDC transmission. The voltage source converter configuration VSC is being applied in the latest developments, and it requires GTOs. Its special properties include the ability to independently control real and reactive power supplied to the ac system, and it does not require an active ac voltage source to commutate unlike the conventional line commutated converter. There is considerable flexibility in the configuration of the VSC converter bridges, and a suitable control system can enhance the system performance.

Before GTOs can be implemented in dc transmission, the series and parallel stacking of the devices and their losses are of major concern in implementing the GTOs for HVDC transmission. At present, however, the GTO ratings are much lower, and their cost and losses are higher compared to a thyristor. With the advent of SiC devices, the three factors mentioned above can be greatly improved, for they have superior material qualities than the Si devices. It is expected that continued research and developments in power electronics would provide exciting new configurations and applications for HVDC converters.

II. MODELING OF SILICON CARBIDE GTO THYRISTOR

To study the impact of a device at the system level and to realize the benefits of using the device, a good device model is required [9], The model is based on the equations derived for power loss in the conduction state and the energy loss during switching on and switching off periods of the GTO thyristor. The developed model has been studied for both silicon and silicon carbide materials and for different ratings of voltages and currents. The device model is presented, followed by simulations to evaluate the switching and conduction losses.

A. Device structure

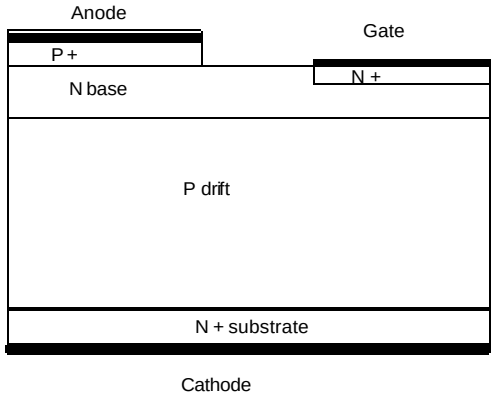


Fig. 1. Device structure of SiC GTO Thyristor used in simulations.

The equations for conduction losses and switching losses are derived in, based on a specific device structure [9], as

shown in Fig. 1. The structure is similar to GTO except for few modifications and has the following features [4].

- The material used is 4H-SiC Polytype.
- The structure has five layers including the 4H-SiC n+ substrate. The second layer is the lightly doped p-type drift layer, followed by lightly doped n-type layer, a heavily doped n-type layer, and finally the heavily doped p-type layer, which carries the metal anode contact. The device has interdigitated anode structure for effective gate control. The N+ doped layer, which forms the base of the upper pnp transistor, has a metal gate contact. Asymmetrical structure – the device can block in only one direction because of the cathode short.
- Complementary pnpn configuration–is complementary to the silicon npnp configuration as explained in the earlier section.
- Heavily doped N+ substrate – due to low resistivity of the p-type SiC
- The lower base thickness is 1.5 times the maximum depletion region width – to accommodate the open base transistor voltage (BV_{ceo}) blocking characteristic of the GTO thyristor. The increase in layer thickness is because of the lower blocking capability of the upper pnp transistor.

B. Conduction losses

The on-state power loss equation is derived as,

$$P_{on\text{-}state} = J.(E_g * q) + J \times \left(\frac{3\pi}{8}\right)\left(\frac{KT}{q}\right) \exp\left(\frac{3.V_B}{2.L_a.E_C}\right) \quad ...(1)$$

In the above equation first term in the sum corresponds to the loss due to the voltage drop across the junction and the second term corresponds to the voltage drop due to on-state specific resistance in the lower base region. This equation can further be simplified and reduced to an expression that is dependent on few parameters [7]. The list of expressions used is,

Then the final expression for conduction losses can be given as,

$$V_B = \varepsilon (N_a + N_d)\frac{E_C^2}{(2.q.N_a.N_d)}$$

$$T_a = T_n + T_p;\ L_a = (D_a + T_a)^{0.5}$$

$$D_a = \frac{2.D_n.D_p}{(D_n + D_p)}$$

$$D_n = \left(\frac{kT}{q}\right).\mu_n,\ D_p = \left(\frac{kT}{q}\right).\mu_p \quad ...(2)$$

Then the final expression for conduction losses can be given as,

$$P_{on\text{-}state} = J.(E_g/q) + J.3\pi.\left(\frac{3\pi}{8}\right)\left(\frac{kT}{q}\right) \exp(D)$$

$$D = (\varepsilon (N_a + N_d).E_C \times 1.5)/(2.q.N_a.N_d.$$

$$\sqrt{kT/q}\ .(\mu_n.\mu_p)T_a/(\mu_n + \mu_p) \quad ...(3)$$

This equation [9] [10] is dependent on doping densities, mobilities, temperature, and applied voltage and current. For a given operating voltage and current, the model behavior varies with temperature, with the doping density fixed for a desired rating of the device.

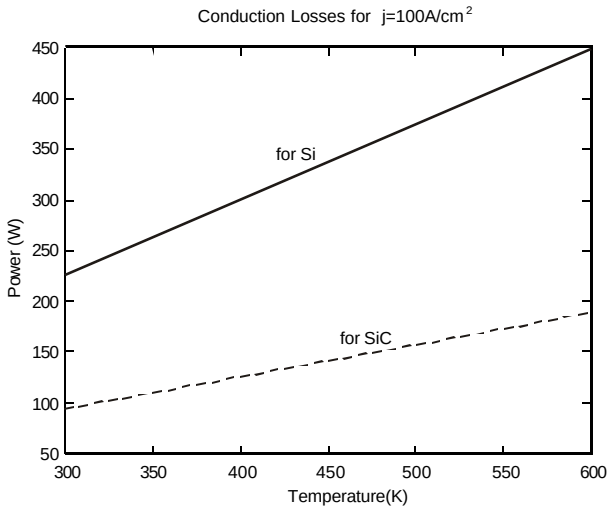


Fig. 2. Conduction losses of Si and SiC GTO thyristor.

Since the electric field for SiC is higher than silicon, which is the dominant factor in the expression, it can be seen that the specific resistance for a silicon device is higher than for a silicon carbide device. Also, for a given operating current, conduction losses vary with the second term in the eq. 1, which is a function of the specific resistance. Hence, the conduction losses are an order higher for the silicon GTO thyristor. Conduction losses for an applied voltage of V= 5000 V and a current density of J = 100 A/cm^2 is shown in Fig. 2. The list of terms used is given in Table 1.

C. Switching losses

The equations for energy losses, during turn-on and turn-off operations, during turn-on, it is assumed that the turn-on gain is very high,

$$V_{off} = \frac{1}{2}\left(e_s.E_c.\frac{V}{1-a_{npn}}\right)\sqrt{\frac{V}{V_B}} + J.a_{npnmax} \times T_a \quad ...(4)$$

$$V_{on} = \frac{1}{3}\left(e_s \cdot E_c \cdot V\sqrt{\frac{V}{V_B}} + j^3 \frac{(3.T.V_B^2)}{e_s . \mu_n E_c^3} \right) + \left(\frac{E_g}{2q} \right) .J.\tau_a \quad ...(5)$$

Hence it can be assumed that the current rise is very fast. During the turn-off period, assuming unity gain turn-off, the energy loss equation is derived as an open base npn transistor turn-off and also assuming that entire anode current flows to the gate terminal [6].

The switching power losses can be calculated using the total energy loss equation as,

$$P_{switching} = (E_{on} + E_{off}) \quad ...(6)$$

Fig. 3 shows the comparison of silicon and silicon carbide devices as the temperature increases for V = 5000 V, J = 100 A/cm^2. There is a noticeable difference between the switching losses of silicon and silicon carbide devices. For the same blocking voltage, thickness of the blocking layer in a silicon device is more than the thickness of blocking layer in a silicon carbide device. The reduction in the blocking layer thickness in silicon carbide devices is because of the high electric breakdown strength of silicon carbide material due to wide band gap.

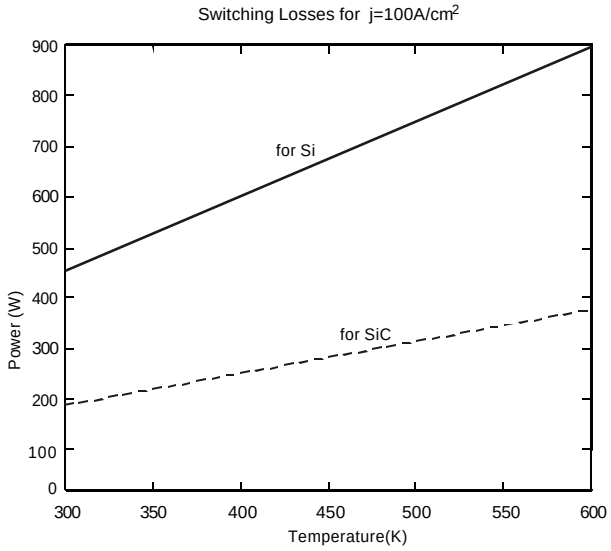


Fig. 3. Switching losses of Si and SiC GTO thyristor.

Thus, the charge stored in the drift region is less, which results in faster switching. Also, the ambipolar diffusion length La, which is a function of ambipolar lifetime, and the electron and hole mobilities for silicon, is greater than silicon carbide due to high carrier mobilities and greater lifetimes. These result in higher switching losses [10]. The additional tail current due to the recombination of residual minority carriers in the base region causes additional power loss during switching. Since there is no additional tail current in a silicon carbide device, the losses are less.

The total power loss in the device is given as,

Total losses = Conduction losses + Switching losses

$$P_{total} = P_{conduction} + P_{switching}$$

The following are details and assumptions made in the development of the model :

- The mobilities and lifetimes of holes and electrons are assumed to beconstant
- The device is doped for a desired breakdown voltage
- The model is studied for variation in temperature for different current and voltage ratings.
- The temperature range is 300 K – 600 K. It should be noted that the silicon GTO cannot withstand more than 423 K; however, the model is tested for comparison purposes.
- The devices are subjected to a current density range of 100 A/cm^2 – 500 A/cm^2.

Table 1: List of terms used in the equations.

K, Boltzmann constant (J/K)	α_{npn} ,average current gain during voltage rise
v_s, electron saturation velocity (cm/s)	R_{sp}, ideal specific on-state resistance (ohm.cm^2)
V_B, break down voltage(V)	N_A, N_D, acceptor and donor concentrations (cm^{-3})
D_a, ambipolar diffusion coefficient (cm^2/s)	$\alpha_{npn,max}$ maximum common base current gain for a given applied voltage
D_n, D_p, electron and hole diffusion coefficients(cm^2/s)	α_{npn} average common base current gain during applied voltage varies form 0 to V
N, electron concentration(cm^{-3})	ε_s, permittivity of the semiconductor(F/cm)
q, electron charge(C)	μ_n, μ_p electron and hole mobility(cm^2/V.s)
E, electric field(V/cm)	T_a, ambipolar carrier lifetime(s)
E_c, avalanche breakdown electric field(V/cm)	T_n, T_p electron and hole lifetimes(s)
E_{on}, E_{off}, turn-on and trun-off losses(J/cm^2)	
J, current density (A/cm^2)	
L_a, L_n, ambipolar and electron diffusion lengths(cm)	
$P_{on\text{-}state}$, on state losses(w.cm^{-2})	
V, applied voltage (V)	

The data used in the simulation is presented in Table 2.

Table 2. List of terms used in the equations

Table 2 : Simulation parameter.

Parameter	4H – SiC	Si
(E_g) Energy gap (eV)	3.2	1.1
ε_r relative permittivity	10.1	11.7
μ_p hole electric field(V/cm)	575e-09	575e-09
E_c critical electric field(V/cm)	2.2 e05	3 e06
τ_n Electron lifetime(s)	1150e-09	1150e-09
μ_n Electron mobility(cm^{-3}/V.s)	900	1360
μ_p Hole mobility(cm^{-3}/V.s)	115	450
V_{sat} saturation velocity(CM/s)	2e07	1e07

The data used in the simulation is presented in Table 2.

D. Simulation of model

The model was simulating with the help of Mat Lab software. The simulation results are shown in Fig. 4. These are few of the many cases simulated and shown for different voltage and current ratings and for different temperatures. The total power loss for the silicon GTO thyristor is more than silicon carbide GTO thyristor for the reasons stated earlier. The trend in the simulation plots is the same for different voltages, currents, and different temperatures. However, there are a few simulations with some ambiguities, which could not be accounted for. The total loss for SiC GTO was increasing with increase in temperature for most of the simulations; however, for certain operating voltage and currents a decrease in loss was observed at certain temperatures

Further analysis of the simulation plots and data reveal that, the model dependency on the parameters such as voltage, current and temperature is split between the conduction and switching loss models. The conduction model is a function of current and temperature, and the switching model is a function of voltage and temperature. Hence, for a change in the operating voltage of the device, there is an increase in the switching losses only and the conduction losses would stay the same.

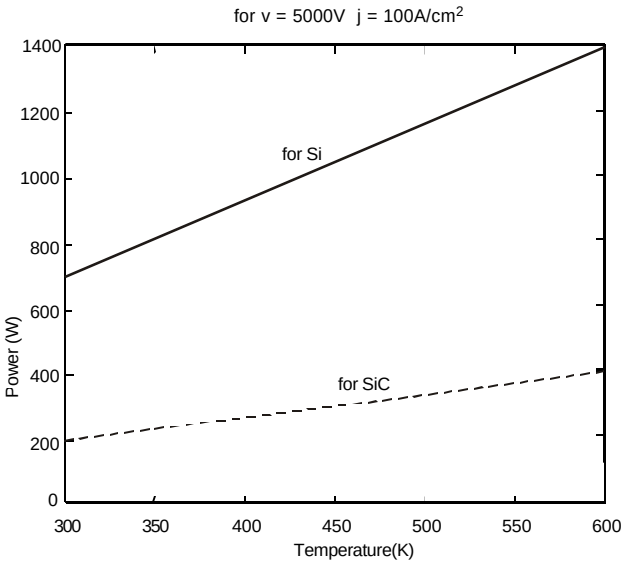


Fig. 4. Device simulation for J = 100 A/cm^2, V = 5000 V

Temperature (K)	P_{Total} Si (W)	P_{Total} SiC (W)
300	669.6	195.48
400	892.4	228.11
500	1115.2	320.74
600	1337.9	383.37

Introduction of a temperature dependent mobility model solved the problem. The equations used in the mobility model are given as,

$$\mu_0 = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{N_a + N_d}{N_{ref}}\right)^{\alpha}}$$

Where $N_A + N_D$ is the total doping concentration, μ_{max} and μ_{min} are the minimum and maximum mobilities of electrons and holes, N_{ref} is the doping concentration for p- type and n-type material calculated empirically and a is the curve fitting parameter, measure of how quickly the mobility changes from μ min to μ_{max} measure of how quickly the mobility changes from μ_{min} to μ_{max}.

III. HVDC SYSTEM

The configuration chosen for the study is a simple mono polar configuration. The transmission system is based on voltage source converter technology. The converter at both ends is a voltage source converter also known as a forced commutated converter [1]. The structure is the same as the basic structure described in the previous section. The system model is designed to emulate the ac characteristics. The main assumption made in the model is that one substation is the sending end and the other is the receiving end

A. System specifications

For Simulation of our system the following specifications are to be used

- System ratings: 120 kV dc link, up to 75 MW power delivered to the receiving end
- Device ratings: SiC - 20kV/ 5kV, 200 A/cm^2, Si – 5kV, 200 A/cm^2
- Number of devices: As discussed earlier, by arranging the devices in series and parallel the converter can handle high voltages and currents. For a rating of 120kV, 1000 A, which is the maximum voltage and current, there are several possible arrangements based on the device rating.

SiC devices : 5 parallel strings of 6 devices in series (for 20kV, 200A device).

5 parallel strings of 24 devices in series (for 5kV, 200A device).

Si devices : 3 parallel strings of 24 devices in series (for 5kV, 400A device).

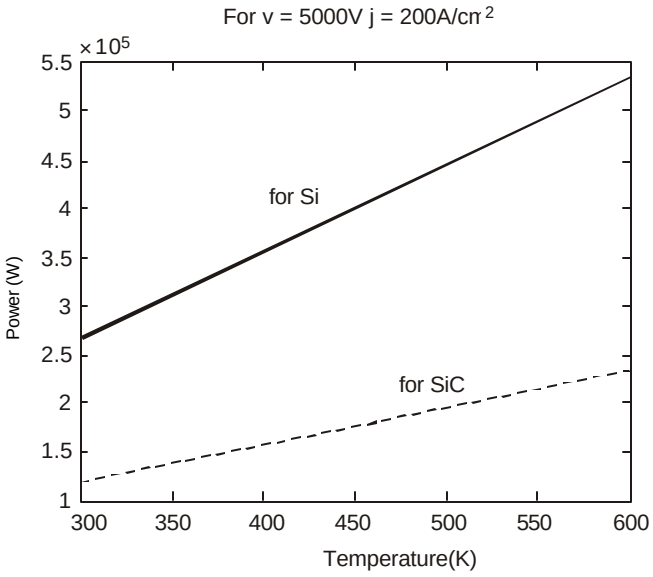
5 parallel strings of 24 devices in series (for 5kV, 200A device).

- The model is tested for a temperature range of 27^o C – 200^o C.

B. Results

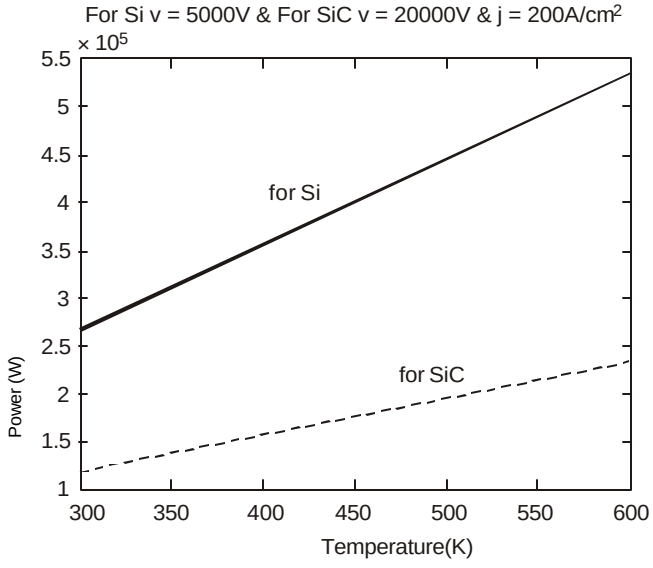
The system was simulating with the help of Mat Lab software. The simulation results for different operating

conditions are presented in figures. The graphs show device voltage and current profiles and the total device losses for a few cycles of the fundamental at different temperatures.



Temperature(K)	Si_{Total}(W)	SiC_{Total}(W)
300	2.6734e+005	1.1684e+005
350	3.1187e+005	1.3617e+005
400	3.5640e+005	1.5549e+005
450	4.0092e+005	1.7481e+005
500	4.4545e+005	1.9413e+005
550	4.8998e+005	2.1345e+005
600	5.3451e+005	2.3278e+005

Fig. 5. System simulation for J = 200 A/cm^2, V = 5000 V.



Temperature(K)	Si_{Total}(W)	SiC_{Total}(W)
300	2.6734e+005	2.0907e+005
350	3.1187e+005	2.4361e+005
400	3.5640e+005	2.7815e+005
450	4.0092e+005	3.1269e+005
500	4.4545e+005	3.4723e+005
550	4.8998e+005	3.8177e+005
600	5.3451e+005	4.1631e+005

Fig. 6. System Simulation for J = 200 A/cm^2, V = 5000 V for Si and V = 20000V for SiC.

As shown in the Fig. 5 & Fig. 6, the losses are a function of the conduction current and vary proportionally with the square of current. The conduction losses are found dominant, similar to the device simulations discussed in the previous chapter. This is because, the switching frequency is low and thus the switching losses are less compared to conduction losses. However, for the same switching frequency, the losses are more for Si GTO than SiC GTO. The total loss of SiC GTO is less than Si GTO as expected, since the on-state resistance of silicon GTO is more than SiC GTO. The losses increase with the increase in temperature due to increase in on-state resistance with temperature. However, the increase in loss, of Si GTO, is more than SiC GTO. These results are used to calculate the efficiency and system cost savings.

IV. EFFICIENCY CALCULATION

The efficiency is calculated based on the power loss profile obtained for different operating conditions. It is the instantaneous loss as a function of the instantaneous current. The plots of power loss for Si GTO and SiC GTO are as shown in Fig. The power loss is different for each cycle as the conduction current duty cycle varies. The maximum and minimum power loss for a single device over a few cycles is measured from the plots, and the corresponding converter controlled switches efficiency is calculated. The efficiency calculations are based on the dc power in the dc link, power loss in the devices, and the number of devices in the converter.

$$\text{Efficiency} = \frac{(\text{dcpower} - P_{loss})}{\text{dcpower}}$$

$P_{loss} = P_{loss}$. (no. of devices in the conveter)

No. of devices = (no. of devices for voltage sharing)
(no. of devices for current dividing)6

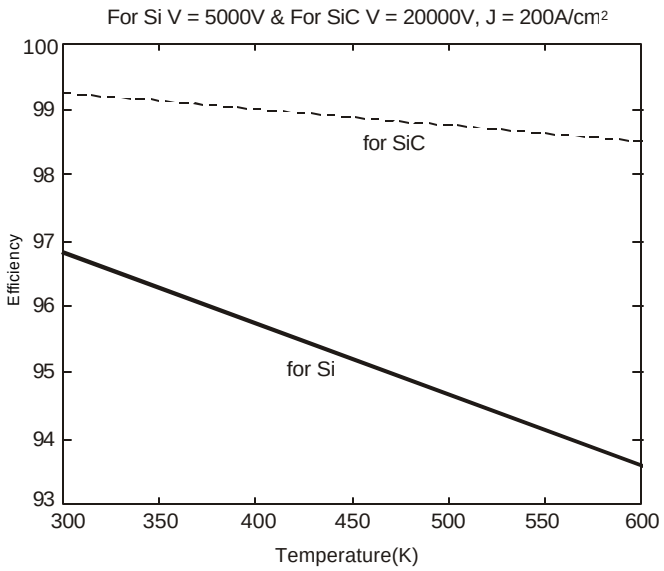


Fig. 7. Converter's controlled switches efficiency plot.

Table 3. Efficiency of SiC & Si GTO converter's controlled switches

Temperature	Efficiency %(Si)	Efficiency %(SiC)
300	96.79839	99.2510
350	96.2647	99.1265
400	95.7311	99.0021
450	95.1975	98.8777
500	94.6639	98.7532
550	94.1303	98.6288
600	93.5967	98.5044

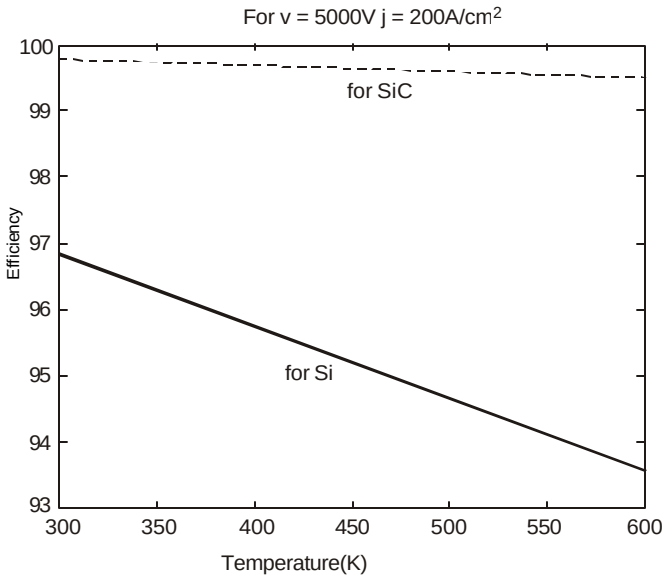


Fig. 8. Converter's controlled switches efficiency plot.

Table 4. Efficiency of SiC & Si GTO converter's controlled switches

Temperature	Efficiency %(Si)	Efficiency %(SiC)
300	96.7983	99.9389
350	96.2647	99.9288
400	95.7311	99.9186
450	95.1975	99.9085
500	94.6639	99.8984
550	94.1303	99.8882
600	93.5967	99.8781

Table 3 show the efficiencies of Si GTO rated at 5 KV, 200 A/cm^2 and SiC GTO rated at 20 KV, 200 A/cm^2. The Fig. 7 shows the efficiency plot for Si GTO and SiC GTO converter's controlled switches. The range of efficiency for SiC converter is higher than Si converter, due to the lesser number of devices and also the average power loss per device is less for SiC GTO. It can also be seen from the plot, that at 27^{o}C, the efficiency is almost the same for the Si converter and SiC converter. However, at higher temperatures the efficiency of the Si converter's controlled switches drops down, but the efficiency of the SiC converter controlled switches is still high. This illustrates that SiC devices can operate efficiently at high temperature. The rating of the Si GTO was changed to study the effect of reduction in number of devices on system performance. Fig. shows the plots of average power for different temperatures.

The voltage rating of the SiC GTO was changed to study the effect of one-to-one replacement of Si GTO with SiC GTO. The SiC GTO is rated at 5kV, 200A/cm^2, so that the number of devices in the converter are equal. Fig. 7 shows that the average power dissipated is much less than compared to 20 kV SiC GTO. This reduction is power loss is because of the reduction in breakdown voltage corresponds to reduction in drift layer width. Hence, for a same diffusion length, the on-state losses are less. Fig. shows the efficiency plot for 5kV SiC. Table 2 shows the efficiency calculation for 5kV SiC GTO. Since the power losses are less, the converter's controlled switches efficiency of 5kV SiC is higher. However, the increase in efficiency is marginal, and the key factor is the number of devices, which determines the installation and operating costs of a converter.

V. SYSTEM COST

The system cost savings is calculated based on the power loss profile obtained for different operating conditions, similar to efficiency calculation. The cost savings was calculated for different ratings of the devices at 100°C.

Calculation:

Difference in losses,

$$dl = (P_{loss\,Si} \,.\, (\text{no. of devices})) - (P_{loss\,SiC} \,.\, (\text{no. of devices}))$$

The converter operates for 365 days and 24 hrs

losses/year = *dl* * 365 * 24

Assuming a rate of Rs. 02/KWHr

Savings = (losses/year) * 02

Table 5 gives the cost savings for a converter using a SiC-based converter with 20 kV, 200 A/cm^2 GTOs instead of 5 kV, 200 A/cm^2 Si GTOs.

Table 5. SiC converter's controlled switches cost savings compared to Si-based converter.

		dI (KW)	Losses/yr (KW)	Losses/yr *2 Rs.
Si 200A/cm^2 for 5000V	Savings	235.55	2063418.0	4126836.0
		274.81	2407335.6	4814671.2
		314.07	2751253.2	5502506.4
		353.33	3095170.8	6190341.6
		392.59	3439088.4	6878176.8
		431.84	3782918.4	7565836.8
		471.10	4126836.0	8253672.0
Si 200A/cm^2 for 20000 V		183.95	1611402.0	3222804.0
		214.64	1880246.4	3760492.8
		245.33	2149090.8	4298181.6
		276.01	2417847.6	4835695.2
		306.70	2686692.0	5373384.0
		337.39	2955536.4	5911072.8
		368.07	3224293.2	6448586.4

The system savings of converter's controlled switches with Si GTO rated at 200 A/cm^2, 20000 V is a little higher compared to 200 A/cm^2, 5000 V Si GTO converter As shown in Table 5, the system savings of converter's controlled switches with Si GTO rated at 200 A/cm^2 is a little higher compared to 400 A/cm^2 Si GTO converter controlled switches. However, the difference in savings is much less. So the advantage of lesser devices overrides the savings because, if the number of devices is less the auxiliary components required will be less and the overall system cost will be reduced. Also, the installation costs will be less and complexity of the system control is reduced to a great extent with the reduction in number of devices. It was also shown in the previous section that the efficiency of a converter with Si GTO rated at 400 A/cm^2 is slightly higher. This illustrates that higher current and voltage rating of a device results in the better performance of the system.

VI. CONCLUSION

Based on the results obtained, a few conclusions can be drawn. SiC devices can withstand high temperature, more than 150^{o}C, and since the losses are also less, thermal management requirements, such as heat sink size, can be greatly reduced. Also, the device operating area (DOA) limits can be improved due to reduced losses, and hence, the maximum frequency can be increased for a given current density and operating voltage. Since the switching losses are less, the switching frequency of the device can be increased which results in improved dynamic characteristics of the system.

Using SiC devices, overall losses can be reduced. Currently, system manufacturers face the challenge of reducing the operating cost of the system and hence demand devices with higher current and voltage rating. It was shown in the study that by using high rated SiC GTO the system savings are improved. Instead of several Si GTOs in series and parallel, fewer SiC devices can be employed for the same rating. Hence it can be concluded that SiC devices close to commercialization can effectively replace the conventional Si based thyristor converters. Even though SiC devices have been realized to have the potential to replace the existing Si devices in power applications, there are few issues to be resolved before SiC can be commercialized. The key issues include material defects like micro pipes, ion implantation, interface, and cost of the material. Also, the increase in rating of auxiliary components and effective packaging techniques are important. Hence, the rate of commercialization depends on development of defect-less material and more importantly the cost of manufacture. At present, however, the GTO ratings are much lower, and their cost and losses are higher compared to the thyristor. The three factors mentioned above can be greatly improved using SiC devices. It can be concluded that continued research and developments in power electronics and power semiconductor technology would provide exciting new configurations and applications for HVDC converters.

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