



Cascaded H-Bridge Multilevel Inverter Using PIC16F877A Controller

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ABSTRACT: Multi-level inverters are emerging as the new breed of power converter options for high power applications. They typically synthesize the stair-case voltage waveform (from several dc sources) which has reduced harmonic content. In this work hardware model of five level single phase cascade H-bridge multilevel inverter has been developed using MOSFET switches. The gating pulses are given to MOSFET switches through the driver circuit. The elimination of harmonics in a cascaded H-bridge multilevel inverter (MLI) by taking the unequal of separated DC sources. A 1-phase, 230V, 0.5HP Induction motor is used as load for testing the developed hardware. Hence the motor run smoothly. Cathode Ray Oscilloscope (CRO) is used to observe the five level staircase output waveform. This five level staircase multilevel inverter reduced the harmonic distortions as compared to two level inverter.

Keywords: Powerconverters, multilevel inverters, Staircase, harmonic

I. INTRODUCTION

In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. Due to many advantages, several topologies for multilevel inverter have been proposed over the years; the most popular being the diode-

clamped, flying capacitor, and cascaded H-bridge structures. The cascaded multilevel inverter consists of a series of H-bridge inverter. The general purpose of this multilevel inverter is to synthesize a desired voltage from several separate dc sources, like batteries, fuel cells, solar cells, and ultra capacitors. Figure 1.1 shows a single-phase structure of a cascade inverter with separate dc sources. Each separate dc source is connected to a single-phase full-bridge inverter. The topology offered two unequal dc sources to generate an equal step five level output is shown in figure 1.

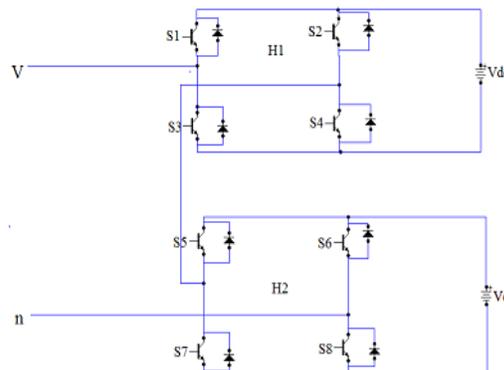


Fig. 1. Cascaded H-bridge multilevel inverter.

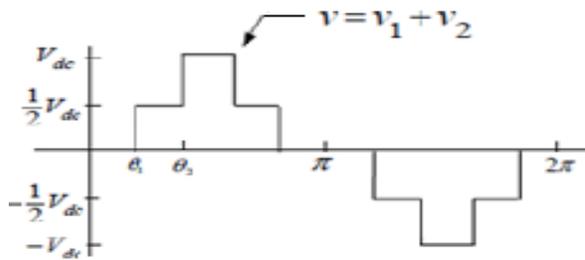


Fig. 2. Output waveform of five level cascaded H-bridge multilevel inverter.

One aspect which sets the cascaded H-bridge apart from other multilevel inverter is the capability of utilizing different dc voltage on the individual H-bridge cells which results in splitting the power conversion amongst higher-voltage lower-frequency and lower-voltage higher-frequency inverters. The primary advantages of

this structures is its simplicity and that fewer or more H-bridge cells can be cascaded in order to decrease or increase the voltage and power level respectively. Today, multilevel inverters are extensively used in high-power applications with medium voltage levels. The field applications include uses in laminators, mills, conveyors, pumps, fans, blowers, compressors and so on.

II. MATERIALS AND METHODS

A. System overview

The block diagram of the proposed cascaded H-Bridge multilevel inverter using PIC16F877A is shown in figure 3. It has single phase rectifier, two H-bridge multilevel inverter, control circuit.

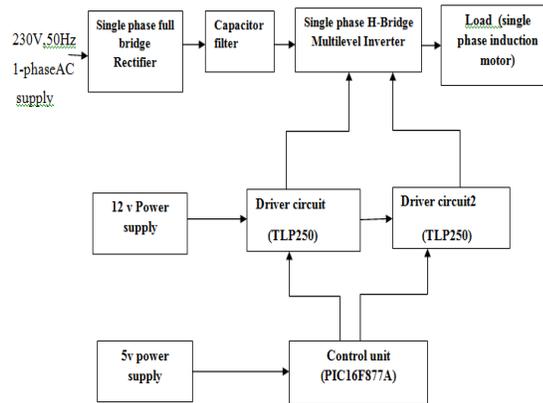


Fig. 3. Block diagram of proposed system.

In the proposed scheme the bridge rectifier is used to provide the dc voltage to the inverter circuit. The full bridge multilevel inverter has IRF 840 MOSFET switches. The inverter is followed by gate drive unit and a control unit. The primary function of the gate drive circuit is to convert logic level control signals into the appropriate voltage and current for efficient and reliable switching of the MOSFET module. In this work an opto-coupler TLP 250 is used to isolate the gate drive circuit and the MOSFET based multilevel inverter circuit. The opto-coupler consists of an infrared light-emitting diode and a silicon phototransistors. The single phase induction motor is fed by cascaded H-bridge multilevel inverter.

B. Power circuit design

The power circuit design contains full bridge rectifier, full bridge inverter assembly. Single phase 230V,50Hz AC supply is applied to the full bridge rectifier. This full bridge rectifier converts single phase AC input into DC. The DC supply is applied to the two cascaded H-

bridge multilevel inverter which is made up of eight MOSFET switches.

C. Control circuit

The control circuit of the proposed scheme consists of PIC 16F877A controller. It is a single-chip embedded controller. The hardware is implemented using the PIC microcontroller PIC16F877A. The advantages of the PIC microcontroller is that the instruction set of this controller are fewer than the usual microcontroller. Unlike conventional processors, which are generally complex, instruction set computer (CISC) type, PIC microcontroller is a RISC processor. The advantages of RISC processor against CISC processor are RISC instructions are simpler and consequently operate faster.

PIC16F877A microcontroller is used to generate triggering pulse for MOSFETs. It is used to control the output of the inverters. Micro controller have more advantage compare then analog circuits and micro processor such as fast response, low cost, small size and etc.

The PIC16F877A belongs to the mid-range family of the PIC microcontroller devices. The program memory contains 14.3K words, which translates to 8192 instructions, since each 14-bit program memory word is the same width as each device instruction. The data memory (RAM) contains 368 bytes. Data EEPROM is 256 bytes. It also consists of two optocoupler for isolating the power and control circuit. All eight MOSFET switches of the power circuit are controlled by the PWM signals generated by the control circuit.

III. EXPERIMENTAL OBSERVATIONS

The proposed control system is designed by a PIC 16F877A based PWM inverter. C language is used to

develop the program. The device is programmed using MPLAB Integrated Developed Environment (IDE) tool. The developed hardware circuit is tested on 1-phase, 230V, 0.5HP induction motor. Hence the motor running smoothly. We observed five level staircase output waveform and also we observed reduction of harmonics in five level multilevel inverter as compared to two level inverter.

The hardware set is developed and tested in power electronics laboratory. The photograph of complete setup is shown in figure 4 and five level staircase output waveform is shown in figure 5. In the complete experiment the crystal ray oscilloscope is used to observe the output waveform.



Fig. 4. Photograph of complete hardware setup.

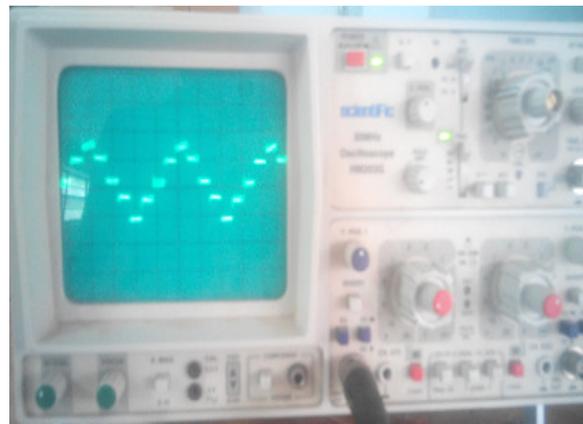


Fig. 5. Output five level staircase waveform.

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CONCLUSION

In this work sinusoidal PWM scheme is used for modulation control. In cascaded H-bridge multilevel inverter separated unequal DC sources are used to generate sinusoidal output. A fundamental switching scheme is used and produces a nearly sinusoidal output. This cascaded inverter design is to get the improved sinusoidal output of an inverter and gives less THD%. The elimination of harmonics in a cascade H-bridge multilevel inverter by considering the inequality of separated dc source. The PWM techniques have been analyzed for the cascaded H-Bridge multilevel inverter. A Micro-controller based gating circuit generates the pulses required by the inverter.

The induction motor drive system is successfully fabricated and tested. This can be important in the high power quality cascaded multilevel inverters which

require several voltage sources and knowledge of the dc voltage levels.

The circuit is tested with a 1-phase, 230V, 0.5 H.P induction motor fed by an MOSFET five level PWM inverter. In this system high performance 8-bit microcontroller with gate driver circuit and additional hardware are present.

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