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A Review of Existing Techniques for Reducing Power Consumption in VLSI Circuits

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ABSTRACT: This paper is to show the survey of how power can be reduced in VLSI circuits in order to give the efficient working of device or system according to demands. As per the versions of Shri. Hrishikesh Kamat, CEO, Shalaka Technologies "optimizing speeds and performances is a challenge." Power consumption is often directly proportional to performance. Higher the power available for consumption, the better will be the performance of the device. But this becomes a problem in bigger devices where lot of power is lost through heat.
So, this paper attempts to review the important techniques used to reduce the power consumption in VLSI design circuits which minimize the amount of leakage current.

I. WHAT IS VLSI?

VLSI stands for "**Very Large Scale Integration**". This is a enormous field which involves packing of electronic devices and minimize the surface area. By the help of VLSI, the electronic circuits that have taken the full space can now put into the small space of few millimeters or centimeters. VLSI makes the unexpected system to work in a possible manner. VLSI circuits have been spread everywhere whether it's your computer, your car, the cell-phones, and whatever you have.

II. CLASSIFICATION

1. Analog: Analog VLSI design is the successful process of Analog circuits and systems using Integrated circuit technology. Such as Amplifiers, Filters, Comparators, Oscillators, Sample-And-Hold Circuits, A/D and D/A Converters, DC-DC converters
2. ASICS or Application Specific Integrated Circuits: The most common application area for this model is DSP - signal filters, image compression, etc.
3. SOC or Systems on a chip: These are the mixture of highly complex signal circuits (digital and analog both on the same chip). A wireless radio chip is an example of an SOC.

III. POWER DISSIPATION IN VLSI DESIGN

In VLSIcircuits' power dissipation are of two types:- Static Power Dissipation and Dynamic Power Dissipation. The power consumption can be expressed by the equation:

PTOTAL= PDYNAMIC + PSTATIC

Power dissipation in circuits is caused by the three major sources:
1. The leakage current which is inherently determined by the fabrication technology. It occurs when system is in standby or in power mode. There are many source of leakage current like source and drain diffusion regions, gate leakage, tunnel current, subthreshold leakage etc.
2. The short-circuit (rush-through) current which is due to the DC path between the supply rails during output transitions.
3. Dynamic power consumption it is due to logic transitions causing logic gates to charge/discharge load capacitance.

IV. NEED OF OPTIMIZATION OF POWER DISSIPATION IN VLSI DESIGN

Power consumption, space and speed are major design parameters in VLSI circuit.These parameters has a major effect on overall performance of VLSI circuits.An optimization of power dissipation can be achieved by compromising various components in designing of circuits. The purpose of reducing the power dissipation in circuits is to maximize the life of systems and fulfill the need of consumer demands by giving extended battery life at lower cost.

The advantage of utilizing a combination of low-power components in conjunction with low-power design techniques is more valuable now than ever before.Modern System-on-Chip demands for more power. In both logic and memory, Static power is growing really fast and Dynamic power kind of grows. Overall power is increasing.

Power dissipation is the main objective when it comes to Portability and smoothness. The mobile-phone consumer demands more features and extended battery life at a lower cost. About 75% of users demand long talk and stand-by time as essential mobile phone feature. The Top 3G/4G requirement for operators is power efficiency. Customers want smaller & sleeker mobile devices. These features requires high levels of Silicon integration in advanced processes, but advanced processes have inherently high leakage current. So there is a need to bother more on reducing leakage current to reduce power consumption.

V. TECHNIQUES OF POWER OPTIMIZATION

Low power has emerged as a principal term in today's world of electronics and communication industries.

The challenges that must be met to designs low power & high performance circuits are as follows-

1. Circuit Level Low Power Design:

(a) Dynamic Power Reductions: There are different ways to low down the power consumption. Clocking system is the dominant contribution of the total power dissipation due to the reason that it has the largest fan-out, highest switching activity (100%), and largest length. These include reducing supply voltage, double edge triggering, and reducing redundant switching.

(b) Leakage Control: As feature size shrinks with scaling, the leakage current increases rapidly, the MTMOS technique as well as transistor stacking, dynamic body biasing and supply voltage ramping can be used to reduce leakage standby power consumption. The main trade are between standby power, invocation overhead, surface area cost, and runtime performance effect.

2. Power Gating designs in Low Power VLSI Circuits: The most trustful approach to low power design is "Power Gating".In a power gating structure, a transistor with high threshold voltage (Vth) is placed in series with a low Vth device and the high Vth transistor is called as the **Sleep Transistor**. In the power gating structure, a circuit operates basically in two modes.

(a) In the active mode, the sleep transistors are turned ON and can be treated as the functional redundant resistances.

(b) In the sleep mode, the sleep transistors are turned OFF to reduce the leakage power.

Among the all leakage reduction techniques, the power gating technique is one of the most supportive method. With the circuit density being increased at small scale, the operation of the sleep transistors plays a vital role in minimizing the leakage power of the circuit.

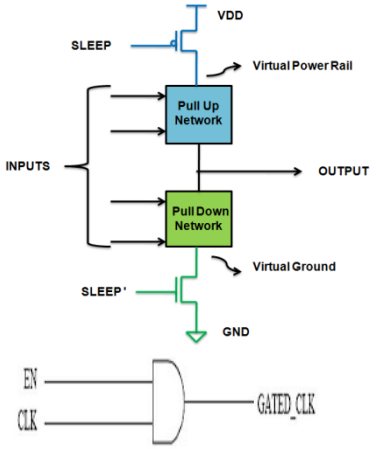

Fig 1. Power Gating [2]

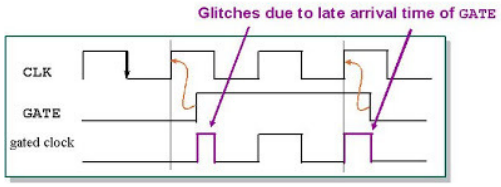

Fig 2. Clock Gating [2]

3. Clock Gating: Clock gating is one of the most widely used power-saving technique used in the Pentium 4 processor and in upcoming next generation processors.

Clock power consumes 50-70 % of total chip power and is expected to apparently increase in the next generation of VLSI designs at 45nm and below as power is directly proportional to voltage and the frequency of the clock

$$\text{Power} = \text{Capacitance} * (\text{Voltage})^2 * (\text{Frequency})$$

Most of the Hardware designers use clock gating to turn off an inactive parts of the design and reduce the overall dynamic power consumption. The RTL (Register-transfer level) approach is important because designers verify power only at the gate level and any change to the RTL needs many design repetitions to reduce power.

4. Sleepy Keeper: For Low-leakage Power VLSI Design, CMOS technology has featured size and threshold voltage for achieving high performance which resulted in increase of leakage power dissipation. Buta

new approach, named "sleepy keeper", reduces the leakage current while saving logic state.

Sleepy keeper uses traditional sleep transistors plus two additional transistors – driven by a gate's calculated output – to save state during sleep mode. Dual Vth (threshold) values can be applied to sleepy keeper to reduce sub-threshold leakage current. Sleepy keeper achieves leakage power reduction with the advantage of maintaining exact logic state. Based on number of experiments with a 4-bit adder circuit, sleepy keeper approach have been achieves up to 49% less delay and 49% less area than the sleepy stack approach.

5. **TBHEX Architecture:** Due to its widespread applications in mobile-phones, and other communication services, low power video codec chip is highly on demand. For motion estimation modification of **Hexagonalblock matching algorithm (BMA)** has been accepted in which TBHEX (*Threshold-basedHexagonal BMA*) has an inherent property of less computational complex, faster throughput, regular data flow and possible to realize with minimum functional blocks . This low power architecture based on TBHEX BMA is termed as TBHEX architecture. By using two on-chip memories (MEMR and MEMC) , the total number of external memory accesses is reduced approximately 88.88%, which in turn reduces the switching activity of the external memory access and thus reduces 88.88% of total switching power dissipated for accessing external memory.

VI. COCLUSION

1. The leakage power is of great concern for designs in VLSI technologies and it is becoming a major contributionto the total power consumption. Leakage power has become more dominant as compared to Dynamic power.
2. The solutions for leakage power dissipation or minimization of leakage power dissipation have to be controlled both by the process of technology and circuit levels.
3. The design for low power has added another benchmark to the complex design problem and the design has to be optimized or reduced for power as well as performance and area.
4. We have studied low-power design techniques, an overview of different low power design methods and ranging from devices to circuits and systems.

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