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Rail-To-Rail Low Power Buffer Amplifier LCD

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ABSTRACT: A high-speed buffer amplifier topology for liquid crystal display driver is proposed. The proposed architecture contains a RAIL TO RAIL common input range, and to output driving stage which is suitable for large and small size liquid crystal display compensation capacitor and resistance are used to enhance the settling time and slew rate of the buffer amplifier an experimental prototype is shown here which is implemented in a .35 µm CMOS technology which draws only 8 µm static current and provide a settling time of 2.8 µs and rising and 3 µs during four the act area for the design of the buffer is 49 *60 µm With power supply of 3.3 it with stand with 1000 pF load capacitance.

I. INTRODUCTION

With increasing demand of high-speed high quality liquid crystal display and market in recent years we have to match with these requirements to fulfill the market demand and LCD driver generally contains shift registers, input register's, data latch, level shifter , digital to analog converter, Pre-Emphasis, and analog buffers the output buffer amplifier is strongly affects the speed, resolution, voltage swing and power dissipation [1,3,4,7]. For each pixel we need a buffer amplifier so as the number of pixel increases the number of buffers to drive to drive the panel increases, nowadays battery operated portable devices are used to increase the performance and to extend the battery life we need low-power high-speed buffer amplifier.

LCD output buffer amplifier are realized by operational amplifier in unity gain configuration generally RAIL TO RAIL operational amplifiers are used to get full output swing RAIL TO RAIL operation amplifiers are consist of complimentary differential amplifiers at first stage and a summing current source at second is stage with generally known as folded cascoded architecture then the output is stage which are this work in class B and class AB.[5,6,9,12,13].

II. RAIL TO RAIL OPERATION

Operational amplifiers are the back bone for many analog circuit designs. It is used in numerous applications such as amplifiers and filters. The operational amplifier can be used in two basic configurations: inverting and non-inverting. These configurations place different requirements on the common-mode input range. The required range varies from almost zero to a full rail to rail. The differential amplifier is used as the input stage for operational amplifiers. The problem is that it will behave as a differential amplifier only over a limited range of common-mode input. Therefore, to make the operational amplifier versatile, its input stage should work for rail to rail common-mode input range. The most common method to achieve this range is to use a complementary differential amplifier at the input stage. This method uses an n-type and a p-type differential pairs simultaneously. Although the method achieves a rail to rail common-mode input operation, it introduces suboptimal operational amplifiers. This is due to the non-constant transconductance (gm) of the complementary differential amplifier. However, there are methods that keep gm variations small over the entire input common mode range [4,5,14,15].

III. THE INPUT STAGE

The input stage of every op-amp is a differential amplifier. In CMOS technology the differential amplifier can be realized using a PMOS or NMOS differential pair. There are several tradeoffs that determine which differential pair to use. One criterion that is considered in making the choice is the common mode input range.

To analyze the common mode input range of the NMOS differential input stage, a simplified diagram will be used as shown in Fig.1. Several modifications are made to the simple differential pair in actual implementation such as active loads and cascodes, however this is sufficient for the purpose of illustration. The range extends from the positive supply to (Vgs, n + VDsat, b) above the negative supply. This minimum voltage is needed to keep the NMOS differential pair and the tail current source in saturation [5,6].

A similar analysis can be carried out for the PMOS differential pair shown in Fig. 2. The range extends from $V_{gs,n}+VD_{sat,b}$ below the positive supply to the negative supply. This minimum voltage is needed to keep the PMOS differential pair and the tail current source in saturation.

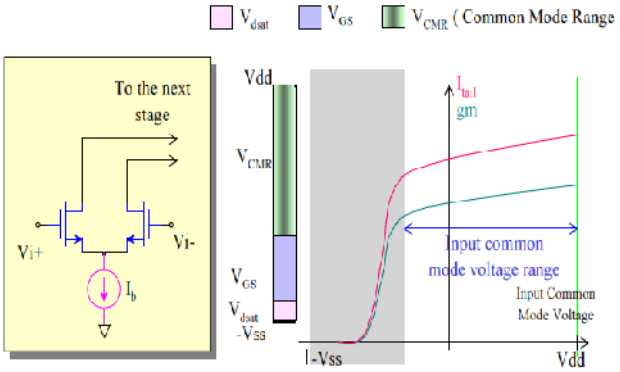

Fig 1. NMOS Differential Pair Common Mode Input Range.

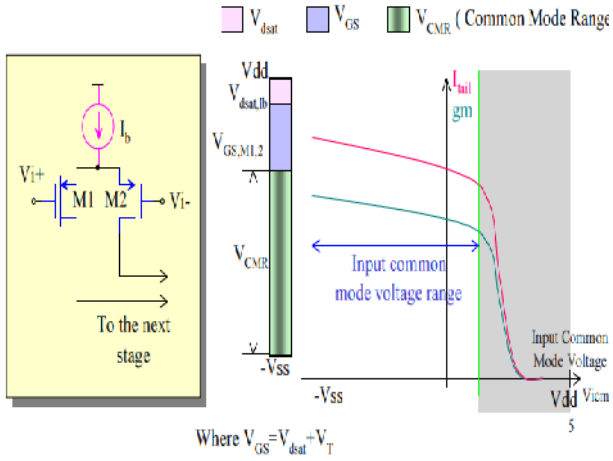

Fig. 2. PMOS Differential Pair Common Mode Input Range.

The simple differential pair cannot meet the rail to rail common mode input requirement. A possible solution to the problem is to use both NMOS and PMOS differential pairs simultaneously. The resulting compound differential pair is called the complementary differential pair and is shown in Figure 3. For low common mode input, the PMOS differential pair is in saturation and NMOS is off. For high common mode input, the NMOS differential pair is in saturation and PMOS is off. Therefore, the total effect is that the complementary differential pair is always working and the rail to rail common mode input requirement is met.

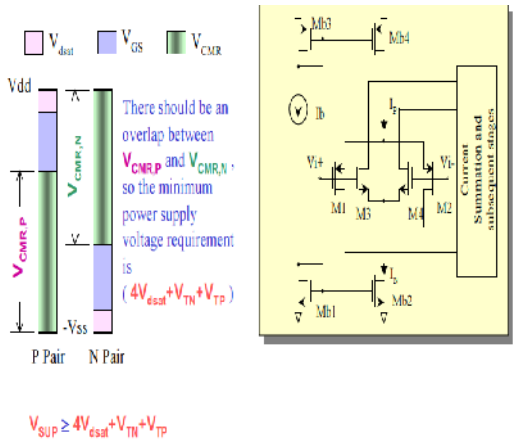

Fig 3. Complementary Differential Pair Common Mode Input Range.

IV. ANALYSIS OF COMPLEMENTARY INPUT STAGE USING DC SHIFTING CIRCUIT TO CHANGE THE INPUT DC LEVEL TO GET CONSTANT Gm

Rail-to-Rail Input Stage, Structure Fig. 4

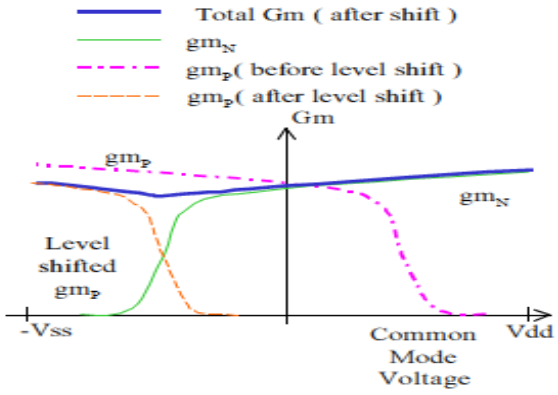

Fig. 4.

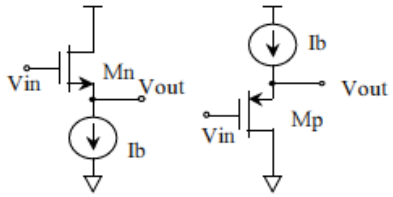

Fig. 4. Transconductance shifting using bias current (DC shifting).

We may notice that there is an overlap between gmN and gmP, so in the middle of the common mode voltage, the transconductance is doubled.

How about shift one of the gm N and gm P curve? And let the transition regions of gm N and gm P come together, so that the total transconductance will be nearly constant among the common mode input range.

Level shift can be implemented by common source voltage follower. We can change the shift level by altering the bias current Ib. Overall schematic with folded cascode structure for DC level shifting fig 5 [18-20].

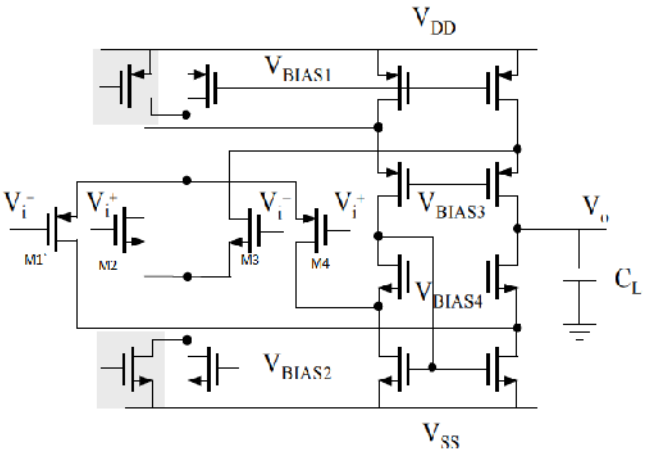

Fig. 5. Rail to Rail folded cascode structure of DC level shifting.

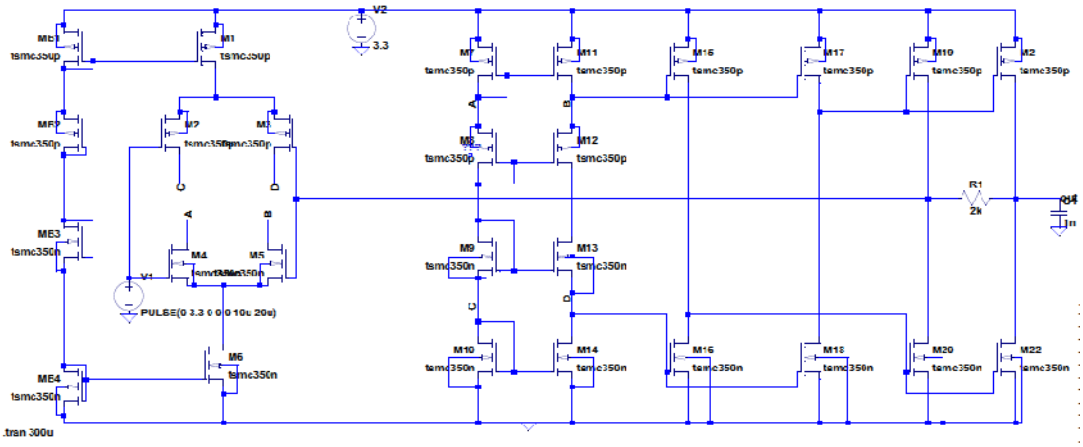

Fig. 6. Schematic of proposed buffer amplifier.

V. PROPOSED BUFFER DRIVING SCHEME

Generally introducing zero in transfer function of buffer amplifier using phase compensation register and output it makes the buffer stable but the slew rate is limited as due to small slew rate the settling time for large capacitive load will increased, means we have to suffer to achieve high-speed. A typical two stage operational amplifier requires compensation for the stability some buffer amplifier's takes the output node as the dominant to achieve the stability without Miller capacitance[3,6] however charge conservation technique is commonly used in some LCD driver to reduce the dynamic power dissipation.

VI. ZERO COMPENSATION TECHNIQUE

Zero compensation technique is generally used to get the dominant pole in buffer amplifier figure 7 shows a buffer amplifier with zero compensation. And fig 8 shows the configuration of proposed buffer amplifier using zero compensation technique. Fig 6 shows the schematic of proposed buffer amplifier.

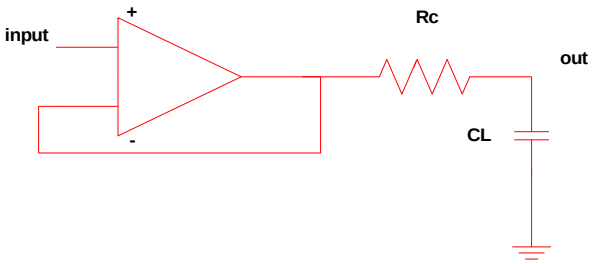

Fig. 7. Zero compensation buffer amplifier.

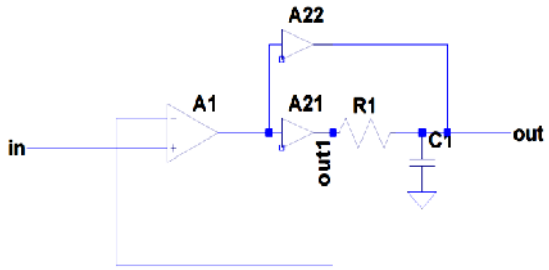

Fig 8. configuration of proposed driving method of buffer.

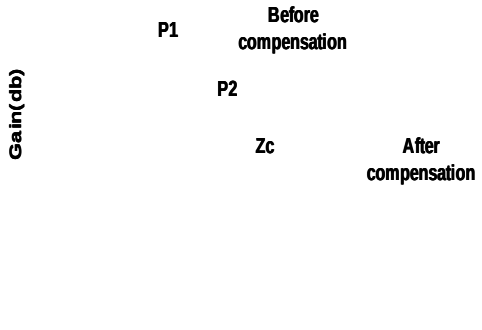

Fig. 9. Frequency response of buffer amplifier with dominant pole.

In figure 9 solid line shows frequency characteristic before compensation and dotted line after compensation, As dominant pole P1 shifted towards origin as with increasing load capacitance means gain bandwidth will decrease it also makes system unstable and degrade phase margin, for proper operation of buffer for high speed phase margin should be in between 70° to 45° generally they prefer 60° phase margin for high speed low-power buffer amplifier design here using "$R_C C_L$" introduces required phase margin, it introduce a zero in transfer function.

$$Z_C = \frac{-1}{R_C C_L}$$

This is called as zero compensation technique for large phase margin, it is generally used when we does not use them Miller capacitor in between differential amplifier and output is stage of differentiated amplifier. The value of zero located to left the most of unity gain bandwidth to the college RGB

$$\zeta = R_C\sqrt{C_L}$$

For 70° phase and margin $\zeta \geq 1$ and amplifier is stable, for $\zeta <$ .6the phase margin is approximately given as I moved to women in

PM ≈ 100 × ζ and settling time = $\frac{4}{\zeta\omega_n}$

To get large phase margin R_C should be large but we can't increase the resistance R_C, so much as it decreases the settling time, so there is compromise in between phase margin and settling time to get optimum phase margin.

As to account large capacitive load we have to increase the biasing current but it will increase the power loss in buffer amplifier, to solve on the issue to account the large capacitive load current dynamic current sensing technique is used to provide extra biasing current only during transition of input signal with the help of voltage divider method the current sensing technique sense the falling and rising edge according to that it provide the extra biasing current**.**

VII. ANALYSIS OF SLEW RATE

In reality the output of the amplifier circuit deviate when input amplitude increases, because the transconductance, conductance and parasitic capacitance depends upon the current flowing in the MOS transistors, and this current does not always the constant it changes when we apply input signal to differential stage, the push-pull stage is generally used as an output stage it is consist of two complementary common source transistors, PMOS and NMOS [13,14].

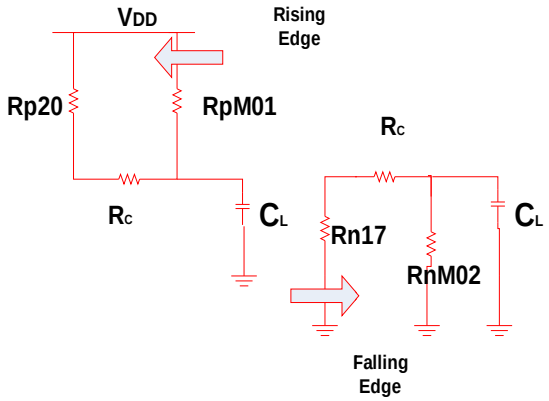

Fig. 10. Large signal equivalent circuit of output is stage for falling and rising edge.

These two transistors are used to charge and discharge the capacitive load. As shown in fig 10.

The output response for rising edge is expressed as:

$$V_{out} = (V_F - V_I)\left[1 - e^{(-t/\tau_p)}\right] + V_I$$

Where VF and VI are the initial and final output voltage and time response is given as:

$$\tau_p = \left[\left(R_{p10} + R_C // R_{pM01}\right)\right].C_L$$

The positive slew rate is calculated as:

$$\left|\frac{dV_{out}}{dt}\right|_{t=t_1} = \left(\frac{V_F - V_I}{\tau_p}\right)\left[-e^{(-t_1/\tau_p)}\right]$$

Similarly the output response at falling is is expressed as:

$$V_{out} = V_F - (V_F - V_I)\left[-e^{(-t/\tau_n)}\right] \quad where$$

$$\tau_n = \left[\left(R_{p17} + R_C // R_{pM02}\right)\right].C_L$$

Negative slew rate can be calculated as:

$$\left|\frac{dV_{out}}{dt}\right|_{t=t_1} = \left(\frac{V_I - V_F}{\tau_n}\right)\left[-e^{(-t_1/\tau_n)}\right]$$

As from the above expressions damping factor ζ depends upon transconductance gm1, and the resistance of MOS using the push-pull output is stage depends upon the current flowing and push-pull stage With the use of dynamic bias sensor , we increase the biasing current during the transition phase of input this results in increase of transconductance gm1 and decreasing output resistance of push-pull stage during charging and discharging with load capacitance, as the settling time depends upon damping factor and natural frequency both this parameters increases with increasing transconductance of gm1 where gm1 is the transconductance of differential is stage, this results and decreasing the settling time means the response of buffer amplifier increases with the use of dynamic bias sensor.

VIII. DESIGN PARAMETERS OF RAIL-RAIL OPERATIONAL AMPLIFIER

process	.35 µm CMOS technology
Power supply	3.3 V
Load resistance	20 kΩ
Load capacitance	1000 pF
power dissipation	1mW
DC gain	60 db
Gain bandwidth product	1 MH
Phase margin	70°
Slew rate	5 V/ µs
Output voltage swing	0-3.3 V
input common mode range	0-3.3 V
Output stage	Class B

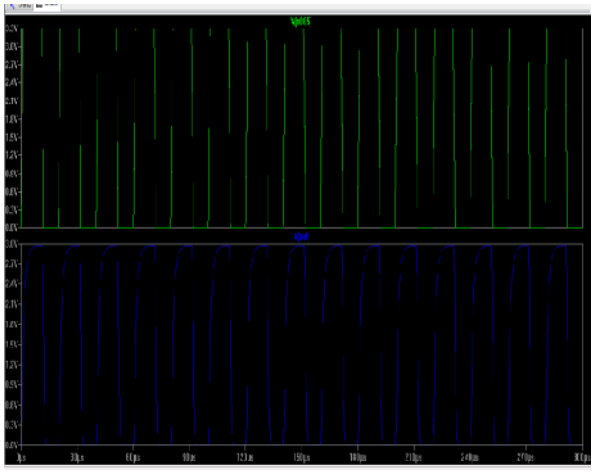

Fig. 11. Simulation result for step response.

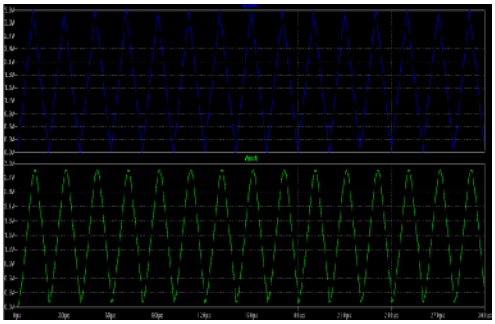

Fig. 12. Simulation result for triangular response.

IX. COMPARISON TABLE

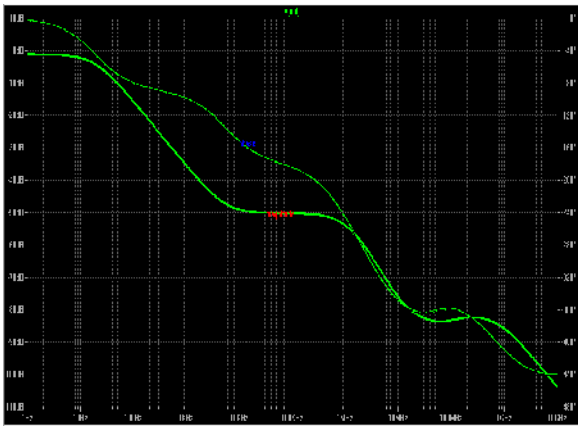

Fig. 13 Block diagram for Frequency response.

	Ref.[20]	Ref.[3]	Ref.[4]	Ref.[1]	This work is
CMOS technology	**.6 µm**	**.6 µm**	**.6 µm**	**.5 µm**	**.35 µm**
Supply voltage	**5 V**	**5 V**	**5 V**	**5 V**	**.33 V**
Max load capacitor	**680 pF**	**170 pF**	**30 pF**	**1000 pF**	**1000 pF**
Quiescent current	**30 µA**	**5 µA**	**8.2 µA**	**32 µA**	**8 µA**
Power	**150µW**	**75 µW**	**150 µW**	**160 µW**	**66 µW**
Settling time	**1.2 µs**	**9.6 µs**	**8.2 µs**	**.7 µs**	**3.2 µs**
Input-output range [V]	**.15/4 V**	**.15/4.8 V**	**.5/4.5 V**	**0/5 V**	**0/3.2 V**
In/out range	**77%**	**93%**	**80%**	**100 %**	**97 %**
Slew rate	**–**	**–**	**–**	**–**	**7 V / µs**
Active area [µm²]	**N/A**	**N/A**	**N/A**	**73 × 91**	**50 ×60**

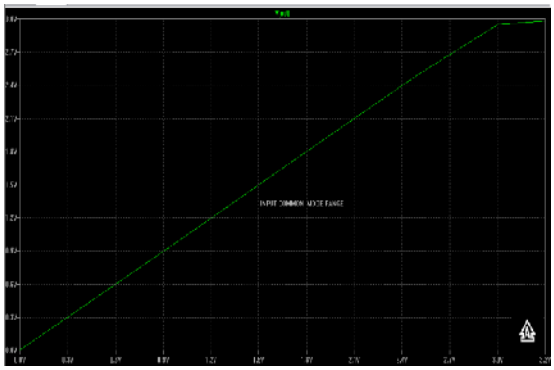

Fig. 14. Simulation result of Input common mode range.

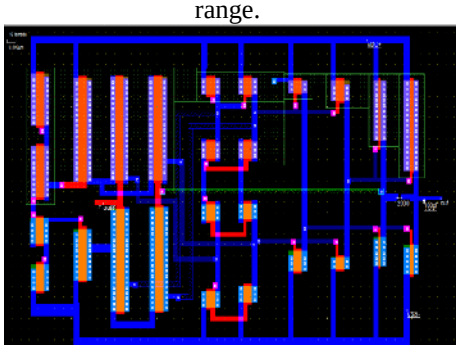

Fig. 15. Layout diagram of rail to rail differential amplifier.

X. CONCLUSION

Self biased high-speed low-power rail to rail buffer amplifier for LCD is proposed work under class B operation which is suitable for small and large size LCD panel, the Zero compensation is used to enhance the slew rate and settling time the compensation resistor value should be optimized to get the optimal value of slew rate and phase margin, as with large value of compensation resistor we get adequate phase margin but it will increase settling time and vice versa. A prototype of this buffer is implemented on .35 µm CMOS technology it draws only is 8 µA static current. The buffer draws little static current but has a large driving capability during transition phase , full swing is obtained by RAIL TO RAIL operational amplifier and enlarge driving capability is obtained by the use of two comparators. The buffer is 3 µs of rising settling time and 3.2 µs of falling settling time, the active area occupied by the buffer is approximately 3600 µm². The performance of the proposed buffer is compared with previous buffer it is superior in power consumption, low static current and small settling time.

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