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Environment Friendly Energy Efficient Counter Design on 28nm FPGA

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ABSTRACT: In green computing field we are always looking to create energy efficient circuit so our computers will consume lees power. Keeping this aspect into the consideration here we have designed our green Johnson Counter which emits low power. In our designed we have tested total power consumption of Johnson counter by taking different range of ambient temperature. At first attempt we have worked at 50 GHz frequency and changed the ambient temperature form 20 °C to 80 °C and found 17.86% of reduction in total power consumption. In second attempt we have worked at 100 GHz frequency and changed the ambient temperature form 20 °C to 80 °C and found 10.71% of reduction in total power consumption. In third we have worked at 250 GHz frequency and changed the ambient temperature form 20 °C to 80 °C and found 5.69% of reduction in total power consumption. In last we have worked at 500 GHz frequency and changed the ambient temperature form 20 °C to 80 °C and found 4.60% of reduction in total power consumption.
We have design our circuit on Kintex 7 FPGA family through VHDL language.

Keywords: Ambient temperature, Low Power, Johnson Counter, 28nm FPGA.

I. INTRODUCTION

Ring counter is a kind of counter which is composed by circular shift register in which output of last flip-flop is becomes input to first flip-flop. Johnson counter is digital circuit, similar to ring counter where numbers of flip-flops are connected in serial manner. But it has very small difference with ring counter is that in Johnson counter input of the first flip-flop is inverted output of last flip-flop.

In Johnson counter if we will use n flip-flop then the MOD of Johnson counter is 2n. If we use Johnson counter instead of ring counter then we required half of flip-flops compared to ring counter for the same MOD.

The one important application of Johnson counter is that it is used to create complicated finite state machine through hardware logic.

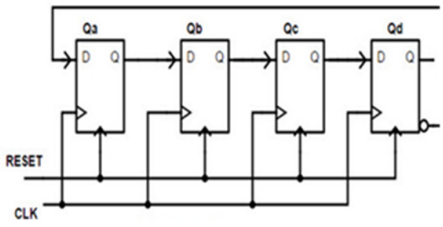

Fig. 1. Circuit diagram of Johnson Counter.

In Fig 1 we have shown circuit diagram of 4 bit Johnson counter through series of D-Flip-Flop and Fig 2 and Fig 3 shown the truth table and timing diagram of Johnson Counter. In figure 4 and 5 we have shown RTL Schematic and Behavioral Model of Johnson Counter.

Q_A	Q_B	Q_C	Q_D
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1

Fig. 2. Truth table of Johnson Counter.

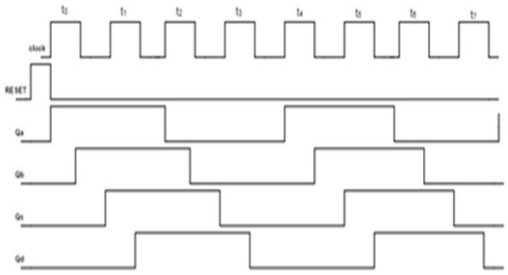

Fig. 3. Timing diagram of Johnson Counter.

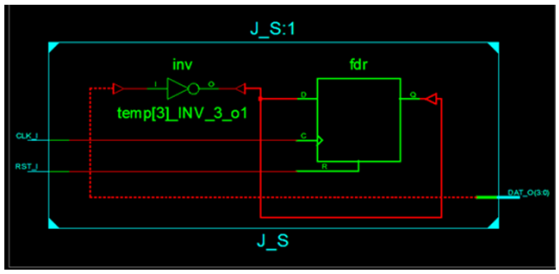

Fig. 4. RTL Schematic of Johnson Counter.

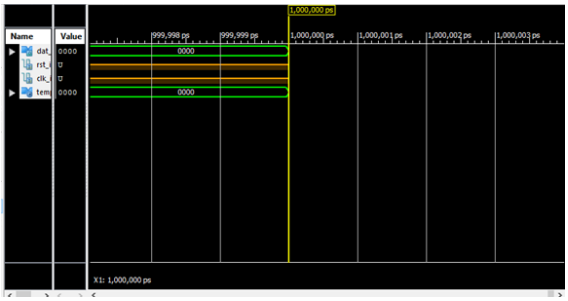

Fig. 5. Behavioral Model of Johnson Counter.

II. Literature Survey

Energy Efficient Counter Design Using Voltage Scaling On FPGA [1], High Performance FIFO Design for Processor through Voltage Scaling Technique [2] HSTL IO Standards Based Processor Specific Green Counter[3]. Leakage Power Reduction with Various IO Standards and Dynamic Voltage Scaling in Vedic Multiplier on Virtex-6 FPGA [4]. Capacitance scaling and frequency scaling were done in order to make energy efficient Image Inverter design [4]. Capacitance scaling was implemented in register to optimize the power dissipation [5] Capacitance Scaling Based Low Power Comparator Design on 28nm FPGA [5]. Energy Efficient CRC Design for Processor of Workstation, and Server using LVCMOS [6].

III. RESULT

We have designed our Johnson Counter on 28nm FPGA Kintex-7 family through VHDL language. For the power analysis we have used the Xpower analyzer tool in Xilnix software.

Table 1: Power Consumption At 50 Ghz.

	Clocks	Logic	Signals	IOs	Leakage	Total
20°C	0.247	0.001	0.009	0.716	0.043	1.016
40°C	0.247	0.001	0.009	0.716	0.069	1.043
60°C	0.247	0.001	0.009	0.716	0.132	1.105
80°C	0.247	0.001	0.009	0.716	0.264	1.237

In table 1 we have worked at 50 GHz frequency and calculated total power consumption with range of ambient temperature (20 °C, 40 °C, 60 °C, and 80 °C). We found that when we change the ambient temperature from 80 °C to 20 °C then there is 17.86% of reduction in total power consumption. Above analysis is also represented by bar graph in Fig. 6.

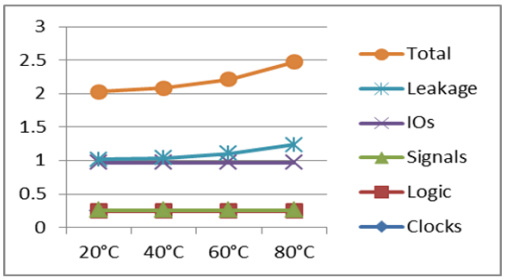

Fig. 6. Power analysis at 50 GHz.

Table 2: Power Consumption At 100 Ghz.

	Clocks	Logic	Signals	IOs	Leakage	Total
20°C	0.494	0.001	0.019	1.433	0.044	1.991
40°C	0.494	0.001	0.019	1.433	0.073	2.020
60°C	0.494	0.001	0.019	1.433	0.141	2.087
80°C	0.494	0.001	0.019	1.433	0.283	2.230

In table 2 we have worked at 100 GHz frequency and calculated total power consumption with range of ambient temperature (20 °C, 40 °C, 60 °C, and 80 °C). We found that when we change the ambient temperature from 80 °C to 20 °C then there is 10.71% of reduction in total power consumption. Above analysis is also represented by bar graph in Fig. 7.

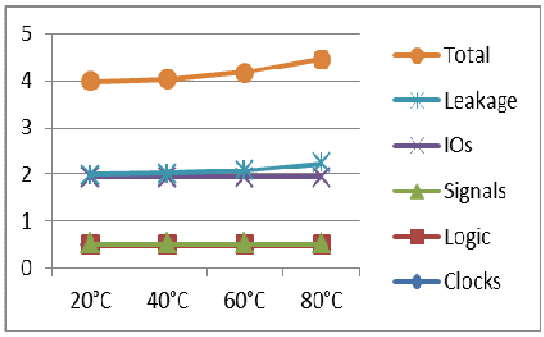

Fig. 7. Power analysis at 100 GHz.

Table 3: Power Consumption At 250 Ghz.

	Clocks	Logic	Signals	IOs	Leakage	Total
20°C	1.235	0.003	0.047	3.581	0.051	4.917
40°C	1.235	0.003	0.047	3.581	0.088	4.954
60°C	1.235	0.003	0.047	3.581	0.174	5.040
80°C	1.235	0.003	0.047	3.581	0.347	5.214

In table 3 we have worked at 250 GHz frequency and calculated total power consumption with range of ambient temperature (20 °C, 40 °C, 60 °C, and 80 °C). We found that when we change the ambient temperature from 80 °C to 20 °C then there is 5.69% of reduction in total power consumption. Above analysis is also represented by bar graph in figure 8.

In table 4 we have worked at 500 GHz frequency and calculated total power consumption with range of ambient temperature (20 °C, 40 °C, 60 °C, and 80 °C). We found that when we change the ambient temperature from 80 °C to 20 °C then there is 4.60% of reduction in total power consumption. Above analysis is also represented by bar graph in figure 9.

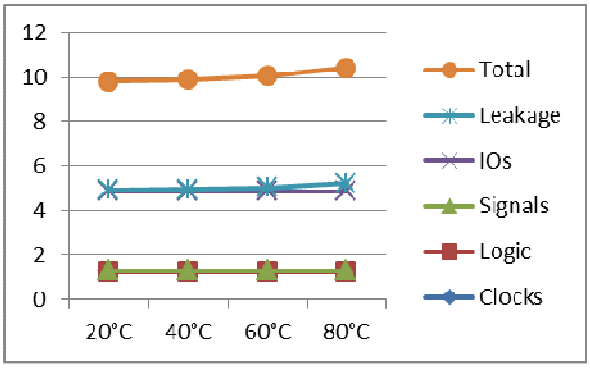

Fig. 8. Power analysis at 250 GHz.

Table 4: Power Consumption At 500 Ghz.

	Clocks	Logic	Signals	IOs	Leakage	Total
20°C	2.470	0.006	0.094	7.163	0.065	9.798
40°C	2.470	0.006	0.094	7.163	0.123	9.855
60°C	2.470	0.006	0.094	7.163	0.246	9.978
80°C	2.470	0.006	0.094	7.163	0.485	10.271

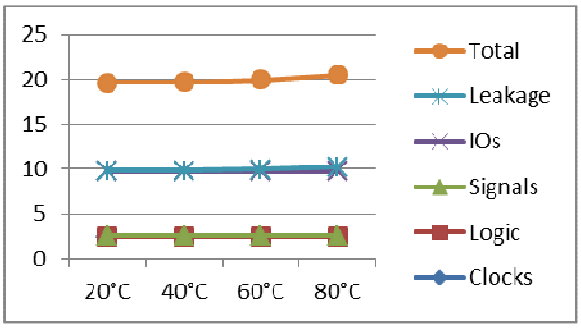

Fig. 9. Power analysis at 500 GHz.

IV. Conclusion

Here we have designed our green Johnson Counter through VHDL language and apply Ambient temperature techniques to calculate total power consumption. In our analysis we have used following (50 GHz, 100 GHz, 250 GHz, 500 GHz) range of frequency at which we change value of ambient temperature and calculate total power consumption of our counter. In our analysis we found that when we changed Ambient Temperature then we got significant change in Leakage power but we got no change with Clocks, Logic, signals, and IOs power.

V. Future Scope

In this work, Green Johnson Counter Design is implemented on 28nm Kintex-7 FPGA family, but we have scope to redesign our Green Johnson Counter with different FPGA family like Virtex 7, Virtex 6, Virtex 5

or we can also apply different- different techniques for calculating total power consumption.

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