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A Reduced Switch Count Multilevel Module Multilevel Converter Topology

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ABSTRACT: In this paper a new multilevel module multilevel converter (MLM-MLI) topology with reduced switch count is proposed. The proposed topology significantly reduces number of dc voltage sources, IGBT switches, switching power losses and gate driver circuitry. A comparative analysis of existing topology and proposed topology has been carried out for eleven level multilevel converter. The analytical analysis and optimization structure of proposed new MLM-MLI and its submultilevel converter is also presented. Operation and performance of proposed eleven level converter topology tested with dissimilar types of multicarrier pulse width modulation (MCPWM) techniques, precisely in-phase disposition (IPD), anti-phase opposition disposition (APOD), carrier overlap (CO) and variable frequency PWM techniques. The results have been confirmed in MATLAB/Simulink in mandate to outstanding the superlative MCPWM technique that gives lowest THD in converter output voltage.

Keywords: Controlling schemes, multilevel inverter, optimal structures, switching states, submultilevel converter and voltage level generation.

Abbreviations: MLM-MLI, multilevel module multilevel inverter; MCPWM, multicarrier pulse width modulation; IPD-LSPWM, in-phase disposition level shifted pulse width modulation; APOD-LSPM, anti-phase opposition disposition level shifted pulse width modulation; CO-PWM, carrier overlap pulse width modulation; VFPWM-variable frequency pulse width modulation; BBBC, bidirectional blocking-bidirectional conducting; UBBC, unidirectional blocking-bidirectional conducting; THD, total harmonic distortion; FFT, Fast Fourier Transform (FFT).

I. INTRODUCTION

Now a days in Power electronics, DC to AC adaptation plays a significant role. Exclusively to extract energy from photovoltaic systems, wind energy and bio fuel cells [1, 2]. The basic concept of multilevel inverter is used to generate staircase wave form by connecting several dc sources in series through semiconductor switches. Thus, the multilevel inverter (MLI) structures were industrialized [3]. It is necessary to use different type of modulation techniques [4] to control output voltage of multilevel inverters and reduce the total harmonic distortion in output voltage of multilevel inverter.

Multilevel inverters are used to produce n number of output voltage levels with large number of switching components. The switching components increases switching losses in inverter and decrease the efficiency of inverter. It necessary to reduce usage of switching components in multilevel inverter. The suggested topology greatly reduces switching components, switching losses and gate driver circuitry compared to traditional capacitor clamped inverters and other conventional inverter topologies [5, 6].

The multilevel inverter slant for dc to ac adaptation suggested numerous Benefits such as [7]. Bidirectional multilevel inverter topology for symmetric and asymmetric structures is reported in [8]. The topologies of [11, 12] point out the drawbacks of cascaded H-Bridge multilevel inverter topology, because of it required large number of switch count and high voltage stress on the device. The improved version of H-Bridge based multilevel converter topology has been presented in [13]. The topology of [14] consist of cascaded connection of submultilevel units with reduced switch count. Optimal design structure of cascaded multilevel inverter and pulse width modulated inverters are reported in [15,16]. The topology in [17] completely reduced the switch count in cascaded multilevel inverters. It produce the numerous voltage levels in inverter output voltage for symmetrical and asymmetrical configurations. Multilevel inverter topology based on hybrid control techniques are presented in [18]. Optimization assessment of multilevel inverters and it analytical analysis is reported in [19]. Similarly, some other upgraded multilevel inverter topologies with reduced switch count have been proposed in [20-25].

II. GENERAL STRUCTURE OF EXISTING TOPOLOGY

The existing topology is also called as MLM-MLI topology [9,10]. This topology presents bidirectional blocking-bidirectional conducting (BBBC) switches for voltage level generation and unidirectional blocking-bidirectional conducting (UBBC) switches for polarity generation. The voltage stress on these switches are not dispersed consistently. Polarity generation switch endure the peak voltage produced by level generation switch. The single-phase multilevel module multilevel inverter (MLM-MLI) structure with contribution of five input dc voltage sources are shown in Fig. 1.

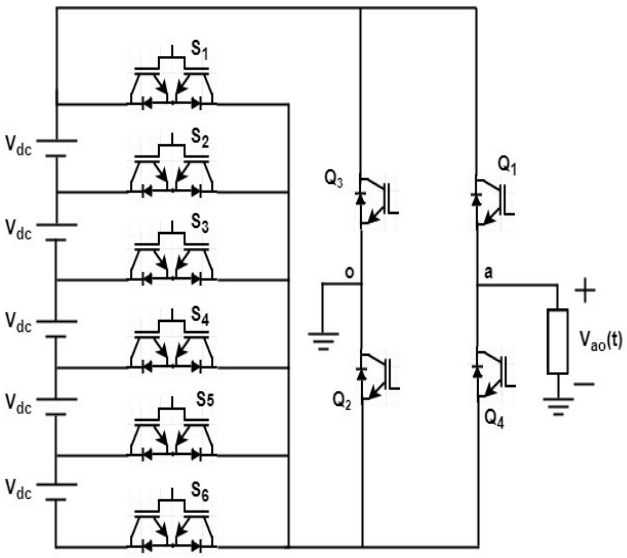

Fig. 1. Existing MLM-MLI Topology [9,10].

The valid operating states for voltage level generation and polarity generation are shown in table 1. This topology is facilitated symmetrical voltage source configuration. That means all five DC voltage sources have same magnitude (V_{DC}). In each state of operation, three switches are conducted. Where one switch from voltage level generation and two switches from polarity generation. Thus in this topology, the polarity-generation switch blocked the maximum voltage stress of $5V_{DC}$ each.

Table 1: Valid Switching States of Existing MLM-MLI Topology.

State	Pole Voltage [$V_{ao}(t)$]	Active Switches
1	$+V_{DC}$	S_2 , Q_1, Q_2
2	$+2V_{DC}$	S_3 , Q_1, Q_2
3	$+3V_{DC}$	S_4 , Q_1, Q_2
4	$+4V_{DC}$	S_5 , Q_1, Q_2
5	$+5V_{DC}$	S_6 , Q_1, Q_2
6	$- V_{DC}$	S_2 , Q_3, Q_4
7	$- 2V_{DC}$	S_3 , Q_3, Q_4
8	$- 3V_{DC}$	S_4 , Q_3, Q_4
9	$- 4V_{DC}$	S_5 , Q_3, Q_4
10	$-5V_{DC}$	S_6 , Q_3, Q_4
11	0	S_1 , Q_1, Q_2

III. STRUCTURE OF PROPOSED TOPOLOGY

Proposed topology is known as a new multilevel module multilevel inverter topology with reduced switch count. Proposed MLM presents reduced switches compared to existing MLM. Existing MLM consist of four UBBC switches for polarity generation in the form of cascaded H bridge and remaining all switches are BBBC switches which are used to generate DC voltage level in converter output voltage. In proposed topology Cascaded H Bridge is completely eliminated and two switches are used for polarity generation.

Where one switch is used for positive polarity generation and another switch is used for negative polarity generation. Proposed topology structure with reduced switch count is shown in Fig. 2.

In proposed topology, Switch S_1 is used for positive polarity generation and switch S_2 is used for negative polarity generation. Switches S_3, S_4, S_5, S_6, S_7andS_8 are used for generating DC voltage level in converter output voltage waveform. Both positive and negative generation. Switches S_1 and S_3 are also used for generating zero voltage level. In proposed topology two switches are conducted in each state of switching but in existing MLM topology three switches are conducted in each state of switching including polarity generation switches. So on state conducting switch count is less in proposed topology which leads to reduce the switching losses in multilevel inverter.

Proposed topology is configured for 11 level inverter and its switching states are shown in table. 2 and structure of switching states of suggested topology is shown in Fig. 3.

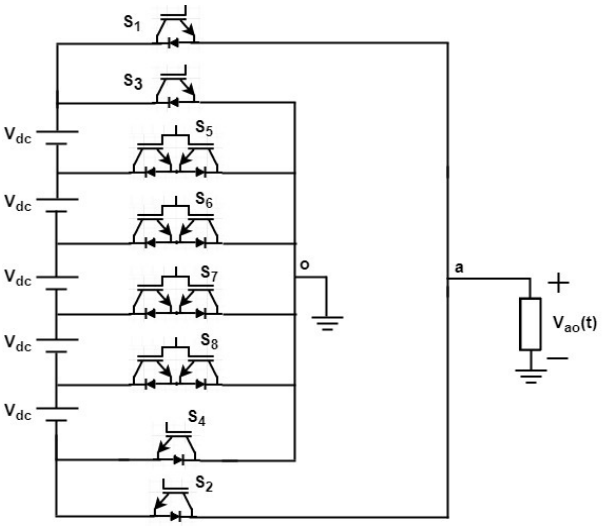

Fig. 2. Proposed MLM-MLI Topology.

Table 2: Switching States of Proposed MLM-MLI Topology.

State	Pole Voltage [$V_{ao}(t)$]	Active Switches
1	$+V_{DC}$	S_1 , S_5
2	$+2V_{DC}$	S_1 , S_6
3	$+3V_{DC}$	S_1 , S_7
4	$+4V_{DC}$	S_1 , S_8
5	$+5V_{DC}$	S_1 , S_4
6	$- V_{DC}$	S_2 , S_8
7	$- 2V_{DC}$	S_2 , S_7
8	$- 3V_{DC}$	S_2 , S_6
9	$-4V_{DC}$	S_2 , S_5
10	$-5V_{DC}$	S_2 , S_3
11	0	S_1 , S_3

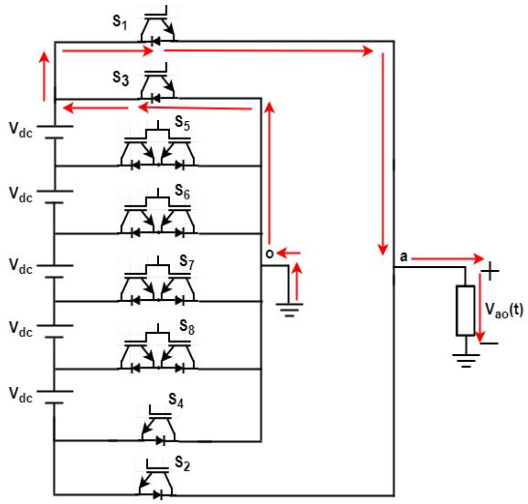

Fig. 3.(a) Zero voltage level generation.

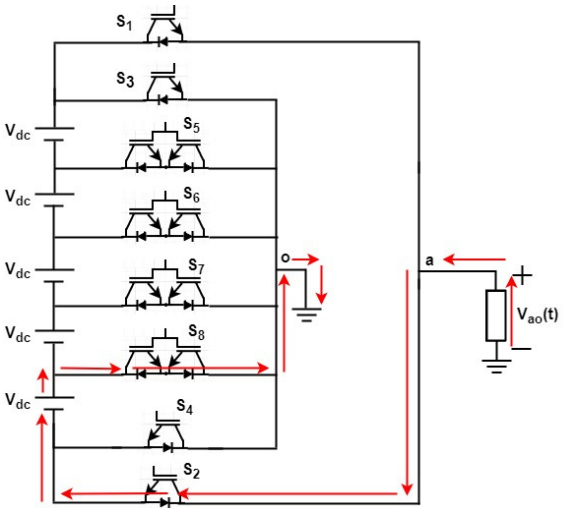

Fig. 3.(d) $-V_{dc}$ voltage level generation.

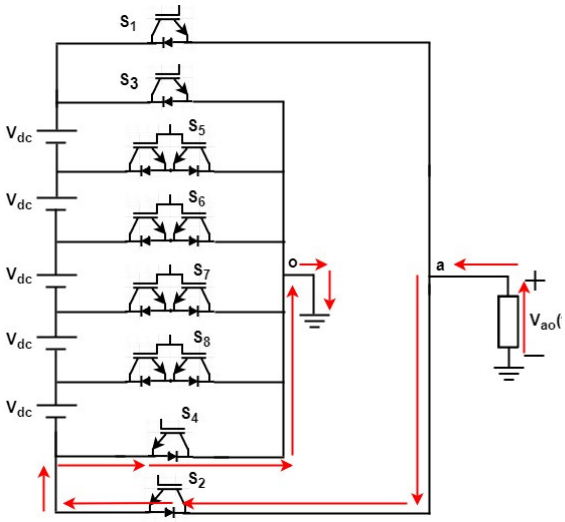

Fig. 3.(b) Zero voltage level generation.

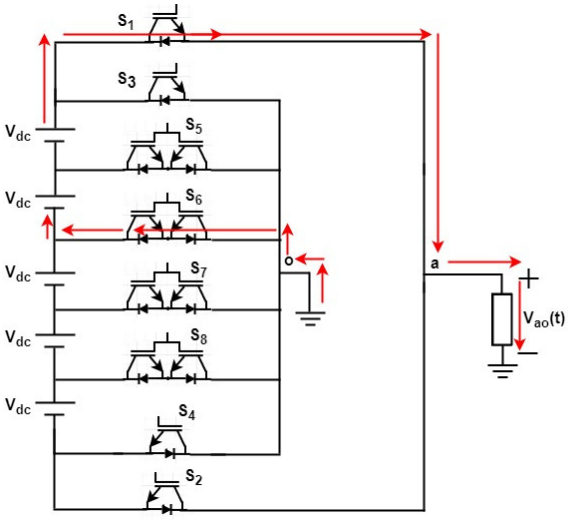

Fig. 3.(e) $+2V_{dc}$ voltage level generation.

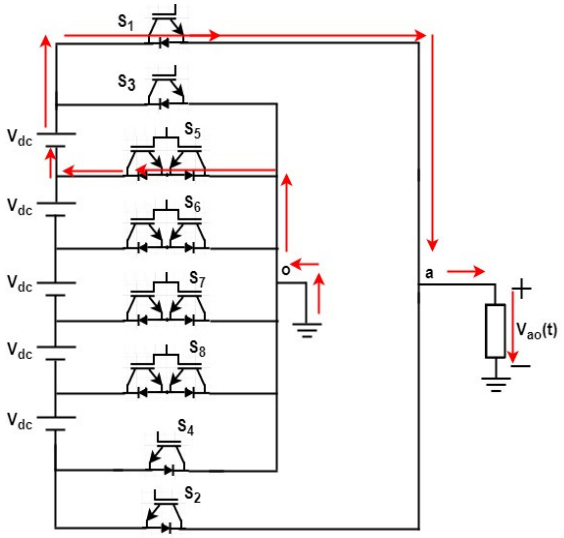

Fig. 3.(c) $+V_{dc}$ voltage level generation.

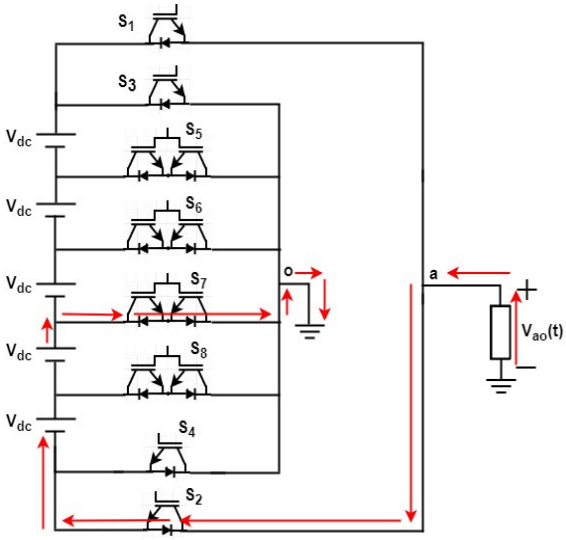

Fig. 3.(f) $-2V_{dc}$ voltage level generation.

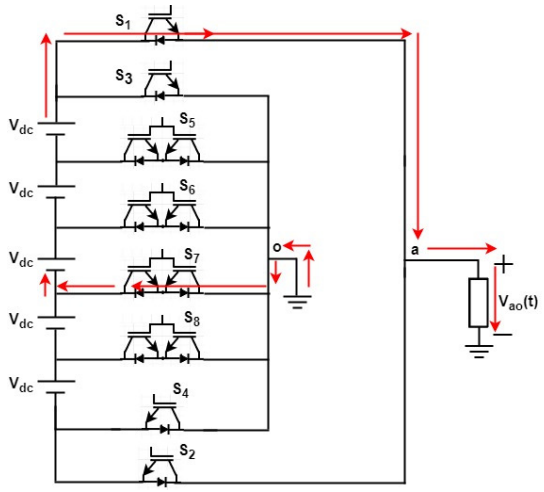

Fig. 3.(g) $+3V_{dc}$ voltage level generation.

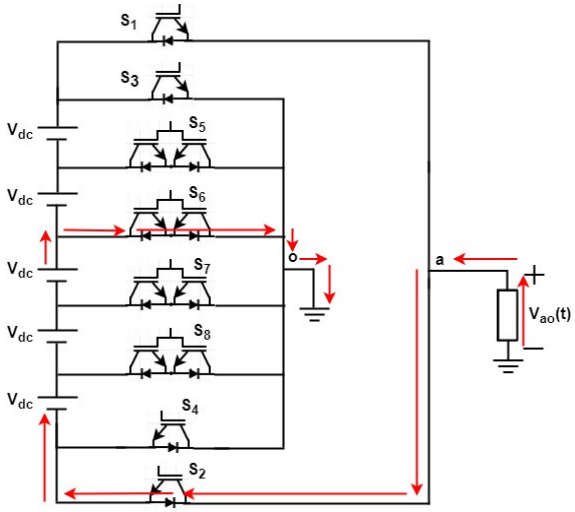

Fig. 3.(h) $-3V_{dc}$ voltage level generation.

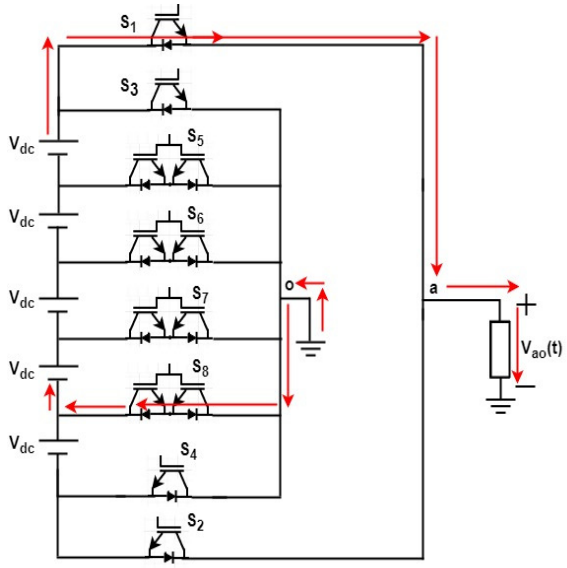

Fig. 3.(i) $+4V_{dc}$ voltage level generation.

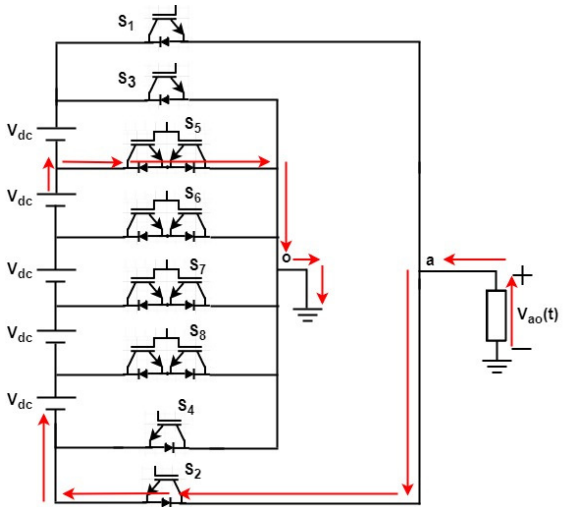

Fig. 3.(j) $-4V_{dc}$ voltage level generation.

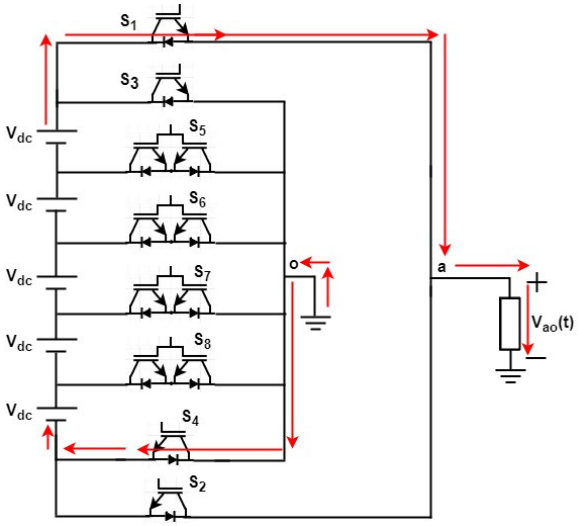

Fig. 3.(k) $+5V_{dc}$ voltage level generation.

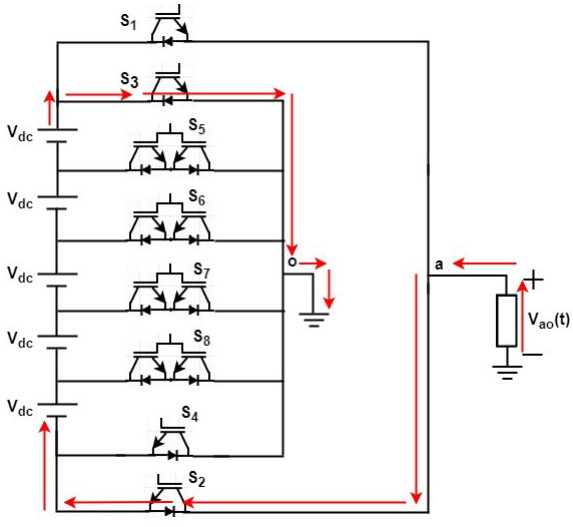

Fig. 3.(l) $-5V_{dc}$ voltage level generation.

Table 3: Differences between Two Topologies for 11 Level Inverter.

Parameter Comparison	Existing MLM Topology	Modified MLM Topology
Total Switches	10	08
Total Polarity Switches	04	02
Bidirectional Blocking-Bidirectional Conducting (BBBC) Switches	06	04
Unidirectional Blocking-Bidirectional Conducting (UBBC) Switches	04	04
N Level (Total Number of Switches for Phase)	(N +1)/2+4	(N - 3)/2+4
N Level (Total Number of Switches for Three Phase)	3(N +1)/2+12	3(N - 3)/2+12

Table 4: Output voltage levels of submultilevel converter.

State	Switches States										V_o
	S_1	S_2	S_3	S_4	S_5	…….	S_{n-3}	S_{n-2}	S_{n-1}	S_n	
1	1	1	0	0	0	…….	0	0	0	0	0
2	1	0	1	0	0	…….		0	0	0	V_1
3	0	0	0	0	0	…….		1	0	1	$-V_1$
4	1	0	0	1	0	…….		0	0	0	V_1+V_2
5	0	0	0	0	0	…….	1	0	0	1	$-V_1-V_2$
⋮ ⋮	⋮ ⋮	⋮ ⋮	⋮ ⋮	⋮ ⋮		⋮ ⋮	⋮ ⋮	⋮ ⋮	⋮ ⋮	⋮ ⋮	⋮ ⋮
2n	1	0	0	0	0	…….	0	0	1	0	$\sum_{i=1}^{n} V_i$
2n+1	0	1	0	0	0	…….	0	0	0	1	$-\sum_{i=1}^{n} V_i$

The comparison between existing topology and proposed topology for eleven level is shown in Table. 3. Proposed topology of submultilevel converter is shown in Fig. 4. This Submultilevel converter is also known as multilevel module (MLM). These submultilevel modules (MLMs) utilized for development of suggested topology. It consists of n number dc voltage sources and n number of IGBT switches, in which (n-4) switches are BBBC switches and 4switches are UBBC switches. It is found that only two switches are conducted to produce each voltage level of MLM. Generation of 2n+1 output voltage level of submultilevel converter is shown in table. 4. Here switches on state denoted by one (1) and switches off state denoted by zero (0).

The suggested reduced switch count multilevel module multilevel converter topology for k number of multilevel modules are shown in Fig. 5. Here n_1, n_2. ….. $n_k$are n number of switches of first MLM to k^{th} MLM respectively. Each submultilevel converter can be produced stepped output voltage waveform by different switching combination. Two switches are used to generate each output voltage level of submultilevel converter. Output voltage of proposed topology with reduced switch count will be obtained between $-\sum_{i=1}^{k}\sum_{j=1}^{n_i} V_{ij}$ and $+\sum_{i=1}^{k}\sum_{j=1}^{n_i} V_{ij}$ by proper selected values of dc voltage sources. Output voltage of suggested topology with submultilevel converter is shown in table. 5. In this topology capacitors can be replaced by renewable energy sources or fuel cells or dc batteries.

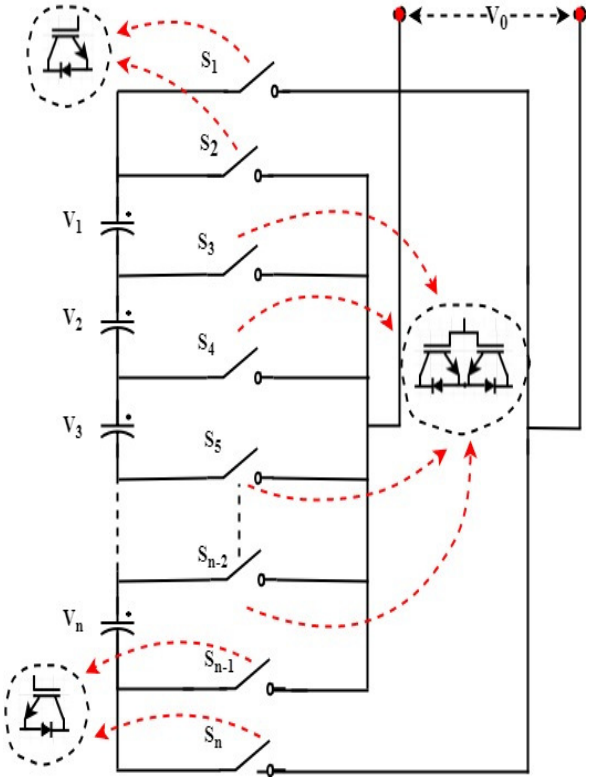

Fig. 4. Submultilevel (MLM) converter of proposed topology.

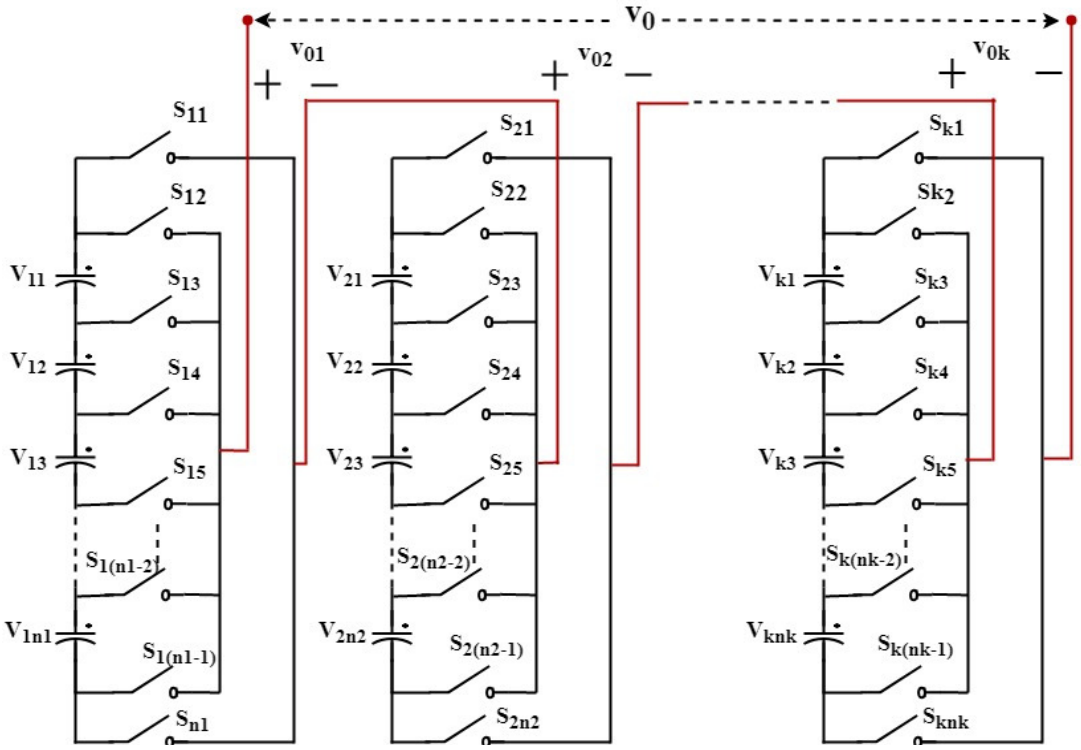

Fig. 5. Proposed multilevel converter topology.

Table 5: Switching states of proposed topology with reduced switch count.

Switching State	Output Voltage (V_o)					
1	S_{11}	S_{12}	.....	S_{k1}	S_{k2}	0
2	S_{11}	S_{13}	.....	S_{k1}	S_{k2}	V_{11}
3	S_{1n1}	$S_{1(n1-3)}$	.....	S_{k1}	S_{k2}	$-V_{11}$
⋮	⋮	⋮	⋮	⋮	⋮	
$2n_1$	S_{11}	$S_{1(n1-1)}$	.....	S_{k1}	S_{k2}	$\sum_{i=1}^{n} V_i$
$2n_1+1$	S_{12}	S_{1n1}	.....	S_{k1}	S_{k2}	$-\sum_{i=1}^{n} V_i$
⋮	⋮	⋮	⋮	⋮	⋮	⋮
$\prod_{i=1}^{k}(2n_i+1)-3$	S_{11}	$S_{1(n1-1)}$	.....	S_{kn_k}	S_{k2}	$+\sum_{i=1}^{n_k} v_{ki}+\sum_{i=1}^{k-1}\sum_{i=1}^{n_i} V_{1i}$
$\prod_{i=1}^{k}(2n_i+1)-2$	S_{12}	S_{1n1}	.....	S_{kn_k}	S_{k2}	$+\sum_{i=1}^{n_k} v_{ki}-\sum_{i=1}^{k-1}\sum_{i=1}^{n_i} V_{1i}$
$\prod_{i=1}^{k}(2n_i+1)-1$	S_{11}	$S_{1(n1-1)}$	.....	S_{kn_k}	S_{k2}	$-\sum_{i=1}^{n_k} v_{ki}+\sum_{i=1}^{k-1}\sum_{i=1}^{n_i} V_{1i}$
$\prod_{i=1}^{k}(2n_i+1)$	S_{12}	S_{1n1}	.....	S_{kn_k}	S_{k2}	$-\sum_{i=1}^{n_k} v_{ki}-\sum_{i=1}^{k-1}\sum_{i=1}^{n_i} V_{1i}$

In this paper, asymmetrical multilevel module multilevel inverter with reduced switch count structure has been studied.

Considering V_{11} as the base voltage

$$V_{Base} = V_{11} = V_{dc} \quad (1)$$

Following algorithm is used to generate output voltage levels of suggested topology and different magnitudes of dc voltage sources are used to generate all output voltage levels. Per-unit system values are denoted, i.e.,

For mode 1

$$V_{dc} = V_{11} \quad (2)$$

$$V_{1i} = V_{11} = V_{dc}, i = 2, 3, \ldots\ldots, n_1 \quad (3)$$

For module 2

$$V_{21} = V_{11} + 2\sum_{i=1}^{n_1} V_{1i} = (2n_1+1)V_{dc} \quad (4)$$

$$V_{2i} = V_{21} = (2n_1+1)V_{dc}, i = 2, 3, \ldots\ldots, n_2 \quad (5)$$

For module 3

$$V_{31} = V_{11} + 2\sum_{i=1}^{n_1} V_{1i} + 2\sum_{i=1}^{n_2} V_{2i} \quad (6)$$

$$V_{31} = (2n_1+1)(2n_2+1)V_{dc} \quad (7)$$

$$V_{3i} = V_{31} = (2n_1 + 1)(2n_2 + 1)V_{dc}, i = 2, 3, \ldots . n_3 \quad (8)$$

In general, for m[th] module

$$V_{m1} = V_{11} + 2\sum_{i=1}^{m-1}\sum_{j=1}^{n_i} V_{ij} \quad (9)$$

$$V_{mi} = V_{m1} = \prod_{i=1}^{m-1}(2n_i + 1)V_{dc}, i = 2,3, \ldots \ldots n_m \quad (10)$$

Maximum value of the output voltage (V_{omax}) of proposed topology is obtained by following equation:

$$V_{omax} = \sum_{i=1}^{k}\sum_{j=1}^{n_i} V_{ij} = \sum_{i=1}^{k}(n_i \times V_{i1}) \quad (11)$$

Following equation is utilized to obtain number of output voltage levels:

$$N_{\text{level}} = \prod_{i=1}^{k}(2n_i + 1) \quad (12)$$

$$N_{\text{level}} = (2n_1 + 1) \times (2n_2 + 1) \ldots \ldots \ldots \times (2n_k + 1) \quad (13)$$

Number of IGBTs in suggested topology can be obtained by following equation:

$$N_{IGBT} = 2(n_1 - 4) + 2(n_2 - 4) \ldots \ldots .2(n_k - 3) + 4k \quad (14)$$

IV. OPTIMAL STRUCTURES

A. Maximum Number of Voltage Levels with constant Number of IGBTS:

Considering (13) and(14) with all are equal in numbers for maximum number of voltage levels.

$$n_1 = n_2 = n_3 \cdots \cdots \cdots = n_k = n \quad (15)$$

Considering (14) and (15),

$$k = \frac{N_{IGBT}}{2(n-4)+4} \quad (16)$$

Maximum number of voltage levels will be obtained by considering the Eqns. (13) and (15),

$$N_{\text{level}} = (2n + 1)^k \quad (17)$$

Using (16) and (17),

$$N_{level} = \left[(2n + 1)^{1/(2(n-4)+4))}\right]^{N_{IGBT}} \quad (18)$$

Using (18), maximum number of voltage levels with constant number of IGBT switches can be obtained.

B. Maximum number of voltage levels with constant number of capacitors:

Considering suggested topology consists of a sequence of *k* number of MLMs and each one consists of n_i capacitors (*i*= 1, 2, . . . , *k*). Thus

$$N_{\text{capacitors}} = \sum_{i=1}^{k} n_i = n_1 + n_2 + \cdots \cdots + n_k \quad (19)$$

Using (15), the number of capacitors can be written as follows:

$$N_{\text{capacitors}} = n \times k \quad (20)$$

Using (17), maximum number of voltage levels can be determined,

$$N_{\text{level}} = \left[(2n + 1)^{\frac{1}{n}}\right]^{N_{\text{capacitors}}} \quad (21)$$

Using (21), maximum number of voltage level with constant number of capacitors can be obtained.

C. Minimum number of IGBTS with constant number of voltage levels:

Considering (14) and (17), as follows:

$$N_{IGBT} = (2(n-4)+4)k = ln(N_{\text{level}}) \times \frac{(2(n-4)+4)}{ln(2n+1)} \quad (22)$$

Using Eqn. (22), minimum Number of IGBTs with constant number of voltage levels can be obtained.

D. Minimum number of gate driver circuits with constant number of voltage levels:

The switches in each MLM of proposed topology assumed to be n, then total numbers of gate drive circuits (N_{driver}) can be obtained, as follows:

$$N_{\text{driver}} = ln(N_{\text{level}}) \times \frac{(n)}{ln(2n+1)} \quad (23)$$

Using (23), for constant N_{level}, minimum number of gate driver circuits can obtained.

V. INVERTER OUTPUT VOLTAGE CONTROLLING SCHEMES

To normalize the inverter output voltage and plummeting the harmonic gratified in inverter output voltage, it must select the most suitable PWM method. In proposed MLM-MLI topology multi carrier sinusoidal PWM (SPWM) technique is functional to the switching devices, in which fundamental frequency of sinusoidal wave modulated with high frequency of triangular carrier wave(s). The generating DC level in inverter output Voltage is based on multi carrier PWM technique. Frequency and amplitude of the multiple carrier signals are diverse constructed on the PWM method. Unique modulation index is continued in all the approaches of multi carrier PWM for assessment. Amplitude of modulation index is the ratio of peak magnitude of reference sinusoidal wave to peak amplitude of high rate of recurrence carrier wave. Rate of recurrence modulation index is distinct as the ratio of carrier wave frequency to reference sinusoidal wave frequency. Notation of Amplitude modulation index and rate of recurrence modulation index are set by Eqn. (24) and (25) correspondingly.

$$M_A = \frac{A_m}{A_c} \quad (24)$$

$$M_F = \frac{F_c}{F_m} \quad (25)$$

Four different type of multi carrier PWM methods are conferred in proposed topology. In all four multi carrier PWM techniques, M_A is continued at 0.9 and M_F is at 40. The fundamental component of the inverter output voltage and THD are detected by MATLAB simulation environment. In all four multi carrier PWM method, bipolar multi carter PWM technique is used. In bipolar multi carrier PWM method, “N-1” high frequency carrier waves are used for “N” numeral of voltage levels.

A. In-Phase disposition level shift PWM (IPD-LSPWM) Method

The high frequency multi carter signals, level are shifted in this pulse width modulation method.

One volt of equal amplitude assigned to all high frequency multi carrier waves and a frequency of 2 kHz is assigned to all carrier waves. The level shifted high frequency multi carter signals are associated with fundamental frequency alignment sinusoidal trend which

is shown in Fig. 6. The dissimilar stages of the output wave is noticed and interpreted to harvest the pulsations which are essential to activate every single switch in the inverter. In directive to acquire three phase inverter structure, the sine trend is phase lifted by 120°.

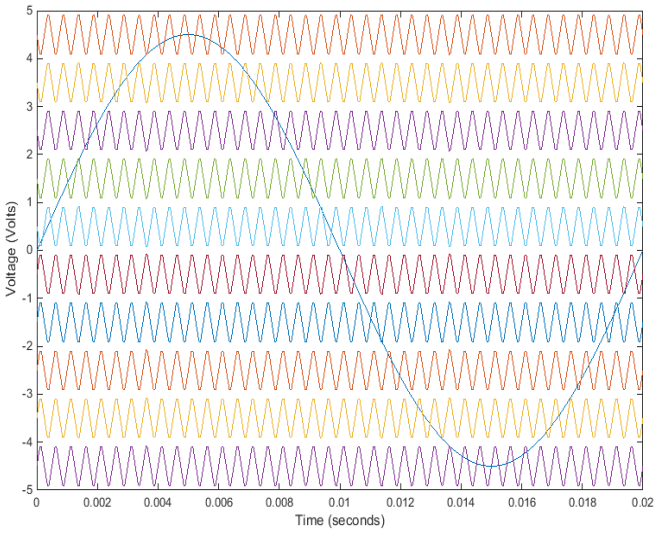

Fig. 6. Modulating Sine Trend and Triangular Trend for IPD-LSPWM at M_A=0.9 and M_F = 40.

B. Anti-phase disposition level-shift PWM (APD - LSPWM) method

Every single high frequency multi carrier signal is 180° phase with adjoining high frequency multi carrier signal. The equal degree of 1 V and rate of recurrence of 2 kHz assigned to all high frequency carrier waves. The high frequency triangular carter signals are associated with the fundamental frequency reference sinusoidal trend which is presented in Fig. 7.

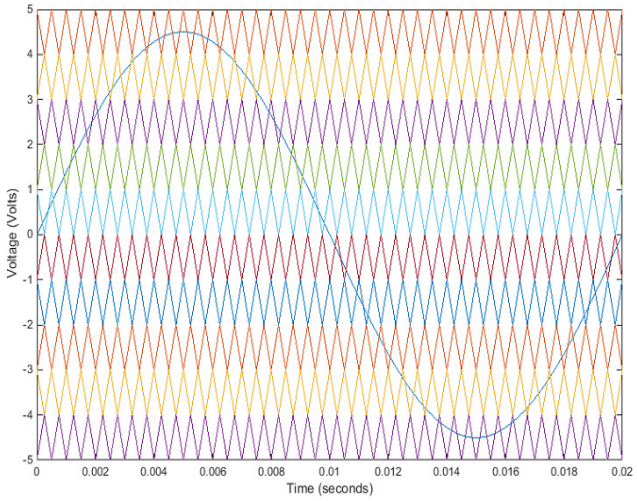

Fig. 7. Modulating Sine Trend and Triangular Trend for APD-LSPWM at M_A = 0.9 and M_F = 40.

C. Carrier overlap PWM (COPWM) method

In this multi carrier PWM method, equal amplitude of one volt and frequency of 2 kHz assigned to high rate of recurrence carrier waves. The high rate of recurrence carrier wave are overlapped and associated with fundamental frequency reference wave. The overlapped multi carrier PWM method is shown in Fig. 8 in directive to harvest the triggering pulses.

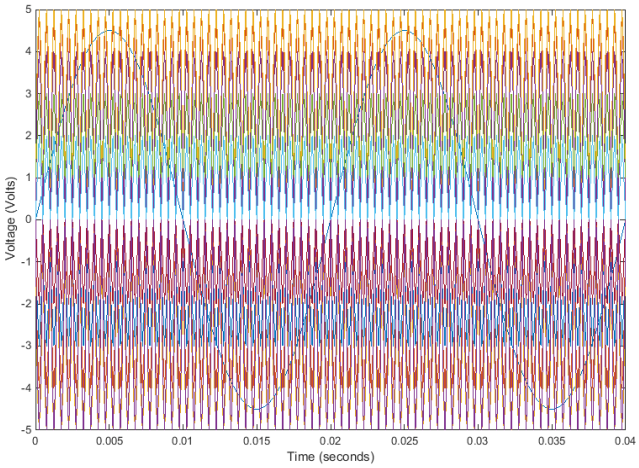

Fig. 8. Modulating Sine Trend and Triangular Trend for CO-PWM at M_A = 0.9 and M_F = 40.

D. Variable frequency PWM (VFPWM) method

In this multi carrier PWM method, equal amplitude of one volt and frequency of 1.5 kHz, 2 kHz, 3 kHz, 4 kHz, 5 kHz are assigned to high frequency carrier waves. Low (1.5 kHz) frequency is assigned to uppermost carrier wave and high frequency (5 kHz) assigned to lower most carrier wave. These high frequency triangular waves are associated with fundamental frequency reference sine wave which is exposed in Fig. 9.

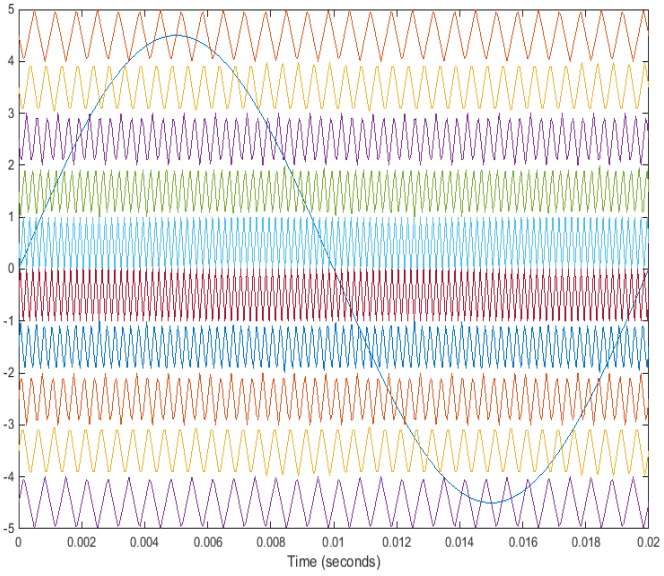

Fig. 9. Modulating reference wave and triangular Wave for VFPWM at M_A=0.9 and M_F = 40.

VI. SIMULATION RESULTS AND DISCUSSIONS

Dissimilar multi carrier PWM performances are functional to the suggested three phase multilevel module multilevel inverter structure. The significance of M_A is continued at 0.9 and significance of M_F is

sustained at 40. A proportional study has been carried out the essential value of inverter peak output voltage and THD by Fast Fourier Transform (FFT) analysis. The topology constraints involved in Simulink model:

$$F_C = 2\ kHz;\ F_m = 50 H_z;\ A_m = 4.5\ V;\ A_c = 5V$$

Three phase Star connected resistive load (per phase resistance R = 50 Ω).
Inverter phase voltage simulation is exposed in Fig.10. In MATLAB simulation five dc voltage sources are connected to invert input terminal. Each and every dc voltage source allotted to voltage of 46 V. The targeted peak voltage is 230 V.

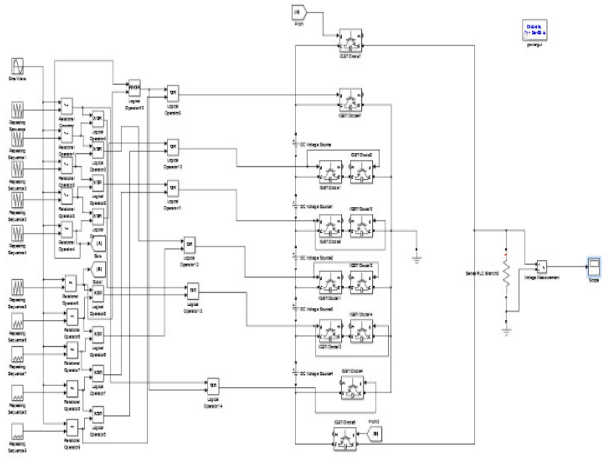

Fig. 10. Simulation of Single Phase 11 Level Inverter Circuit.

Inverter voltage and it harmonic content by using FFT analysis is carried out for in-phase disposition level shifted multi carrier PWM is shown in Fig. 11 and 12. In IPD-LSPWM, 10 triangular carrier waves with 2 kHz frequency modulated with 50 Hz frequency of sinusoidal reference wave.

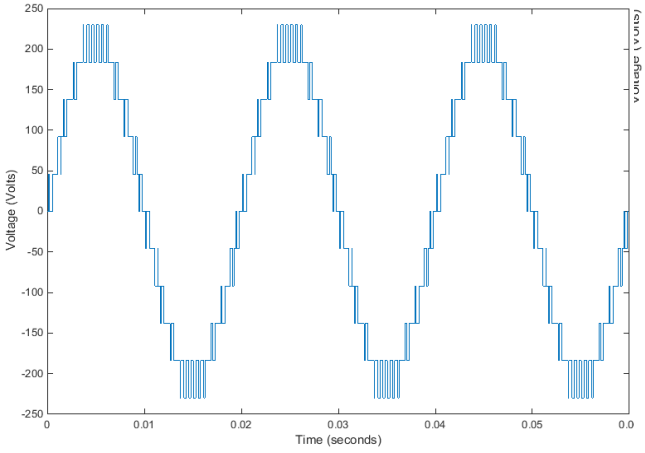

Fig. 11. Eleven (11) Level Proposed MLM-MLI Inverter Voltage in IPD-LSPWM Technique.

The generated gate pulses are applied to switching devices of MLM-MLI. From simulation results, 230 V peak voltage and total harmonic distortion (THD) of 13.30 % is observed from FFT analysis in inverter output voltage.

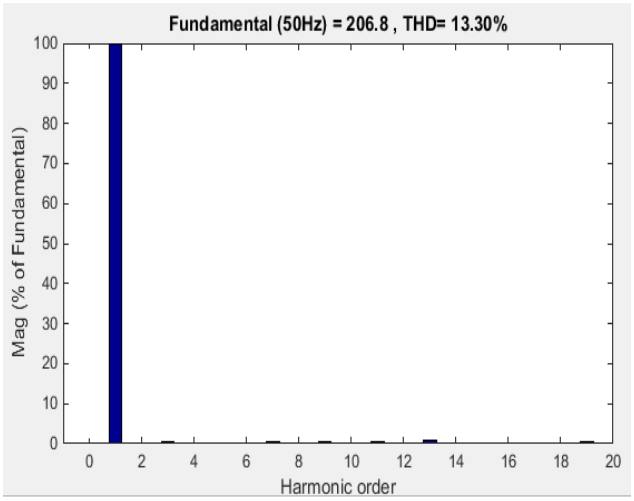

Fig. 12. Harmonic Examination for IPD-LSPWM Technique.

Inverter voltage and it harmonic content by using FFT analysis is carried out for anti-phase disposition level shifted multi carrier PWM is presented in Fig. 13 and 14. In APD-LSPWM, 10 triangular carrier waves with 2 kHz frequency and 180° phase shift of one and other triangular carrier wave modulated with 50 Hz frequency of sinusoidal reference wave. The generated gate pulses are applied to switching devices of MLM-MLI. From simulation results, 230 V peak voltage and total harmonic distortion (THD) of 14.21 % is observed from FFT analysis in inverter output voltage.

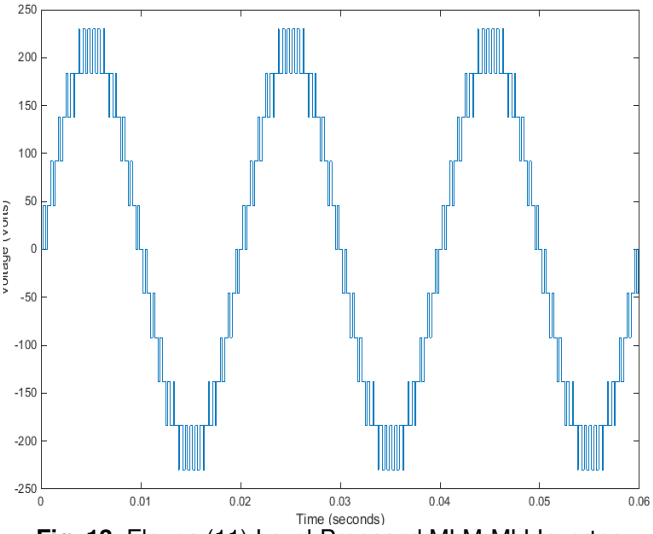

Fig. 13. Eleven (11) Level Proposed MLM-MLI Inverter Voltage in APD-LSPWM Technique.

Inverter voltage and it harmonic content by using FFT analysis is carried out for carrier overlap PWM is exemplified in Fig.15 and 16. In CO-PWM, 10 overlapped triangular carrier waves with 2 kHz frequency modulated with 50 Hz frequency of sinusoidal reference wave. The generated gate pulses are applied to switching devices of MLM-MLI. From simulation results, 230 V peak voltage and total harmonic distortion

(THD) of 37.21 % is observed from FFT analysis in inverter output voltage.

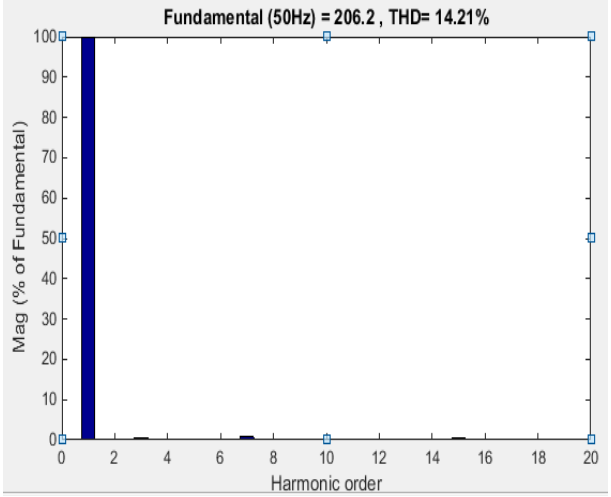

Fig. 14. Harmonic Analysis for APD-LSPWM Technique.

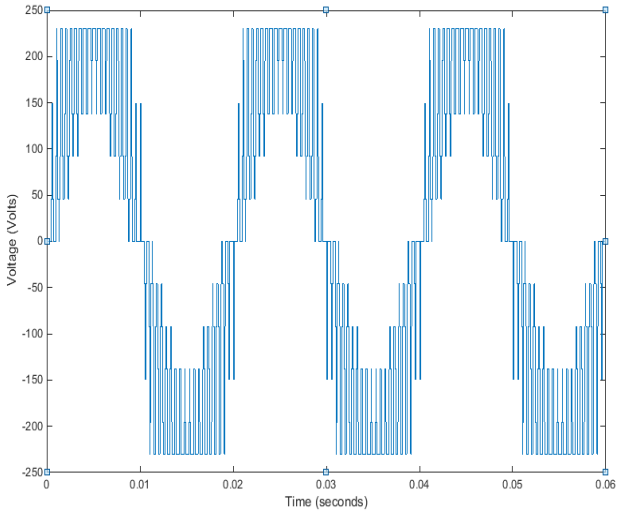

Fig. 15. Eleven (11) Level Proposed MLM-MLI Inverter Voltage in CO-PWM Technique.

Inverter voltage and it harmonic content by using FFT analysis is carried out for variable frequency PWM is shown in Fig.17 and 18. In VF-PWM, 10 triangular carrier waves with variable frequency of 1.5 kHz, 2 kHz, 3 kHz, 4 kHz and 5 kHz modulated with 50 Hz frequency of sinusoidal reference wave. The generated gate pulses are applied to switching devices of MLM-MLI. From simulation results, 230 V peak voltage and total harmonic distortion (THD) of 13.10 % is observed from FFT analysis in inverter output voltage. Three phase MLM-MLI phase voltages and line voltage are presented in Fig. 19 and 20. In three phase MLM-MLI simulation, variable frequency PWM technique is used. In this control technique, 10 triangular carrier waves with variable frequencies of 1.5 kHz, 2 kHz, 3 kHz, 4 kHz and 5 kHz modulated with 50 Hz frequency of reference sine wave. Generated gate pulses are applied to switching components of inverter circuit for R-phase. Y-phase and B-phase inverter circuit gate pulses are generated by shifting the reference sine wave by 120° and 240°.

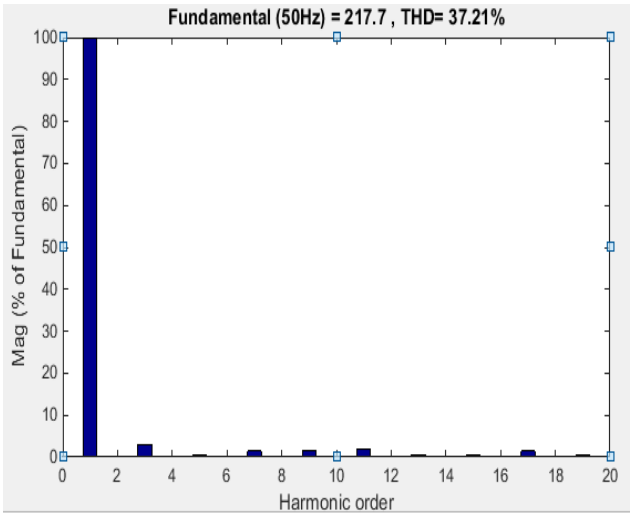

Fig. 16. Harmonic Study for CO-PWM Technique.

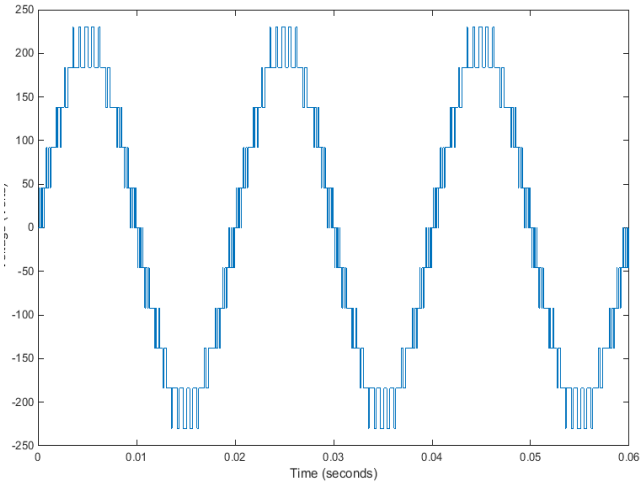

Fig. 17. Eleven (11) Level Proposed MLM-MLI Inverter Output Voltage in VF-PWM Method.

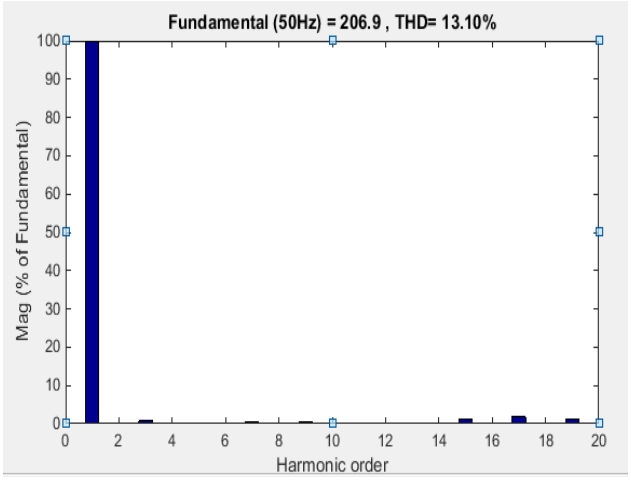

Fig. 18. Harmonic Investigation for VF-PWM Technique.

Generated gate pulses are applied to Y-phase and B-phase inverter circuits. From simulation results, 230 V peak voltage and 400 V line voltage are observed for star connected resistive load of 50 Ω per phase. This three phase inverter circuit is also tested with resistive-inductive (R = 50 Ω and L = 50 mH) load.

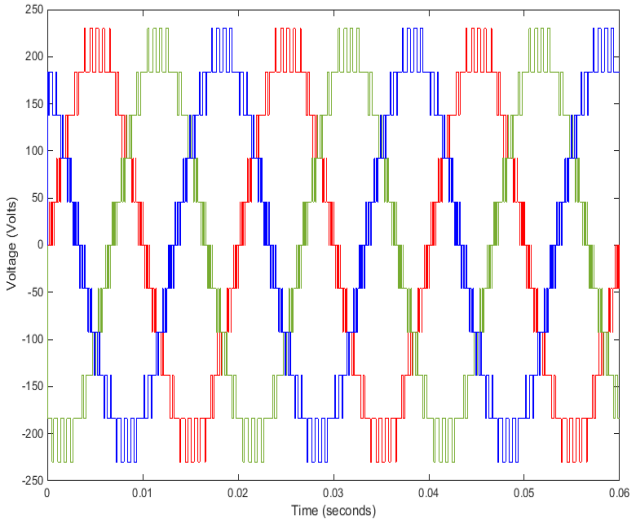

Fig. 19. Proposed MLM-MLI Three Phase Voltage Waveform.

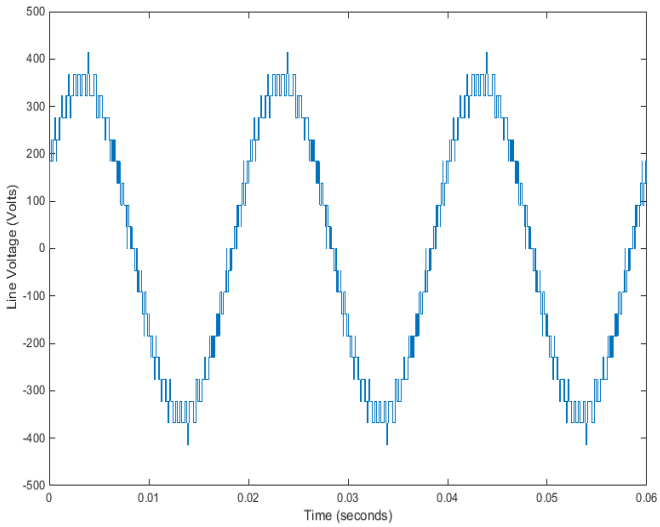

Fig. 20. Line Voltage Waveform for Proposed MLM-MLI Topology.

Table 6: Harmonic Spectrum Comparison for different MCPWM Techniques.

S.NO.	Peak Value of Inverter Output Voltage(Volts)	PWM Scheme	Total Harmonic Distortion (THD in %)
1	230 V	IPD-LSPWM	13.30
2	230 V	APD-LSPWM	14.21
3	230 V	CO-PWM	37.21
4	230 V	VF-PWM	13.10

The performance analysis of all four PWM methods of proposed MLM-MLI inverter topology for THD and peak value of output voltage is presented in Table 6. From all four methods, VF-pulse width modulation method is given minimum harmonics spectrum in inverter output voltage.

VII. CONCLUSION

In this paper an improved version of multilevel module multilevel inverter topology is presented. The proposed topology reduces switching components, switching losses and gate driver circuitry compared to existing topology. Analytical analysis and optimal structures of proposed topology is analyzed for n-levels. The proposed topology simulation has been carried out for eleven level inverter and it also compared with existing eleven level inverter topology. Output voltage of eleven level inverter topology and its harmonic spectrum have been evaluated with different types of multicarrier PWM techniques. From simulation results, it confirmed that, variable frequency pulse width modulation (VFPWM) offers lowest (13.10%) total harmonic distortion (THD) in eleven level inverter output voltage.

VIII. FUTURE SCOPE

The proposed topology required $\frac{n-1}{2}$ capacitor for n-levels. These capacitors are unequally charged to input dc voltage. So that, the future work of this topology will be balancing the capacitor voltages for n-levels.

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