

## Analysis of Performance of Switched Capacitor Circuits

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**ABSTRACT:** In switched capacitor circuits, it is quite common to use MOSFET switches, integrated capacitors (IC) and non-overlapping clocks for carrying out switching operations. MOSFET switches are far from ideal switches mainly when they are operated with small operating voltages. Some investigations have been carried out on the performance of switched capacitor resistors (SCRs) with the switches operated under varied conditions. Further, an attempt has been made to find out how closely SCR represents conventional resistors. It has been found that the SCRs with ideal components satisfy the properties of series and parallel connected conventional resistors. Further, the energy dissipation in SCR is the same as that in conventional resistors when operated under fixed voltage difference. FET based SCRs exhibit higher resistance values, compared to SCRs with ideal switches depending on the operating conditions. When SCRs are loaded with conventional resistors or capacitors, their output is entirely different from those, where only conventional components are used. This paper aims to describe the efforts made to find out the limitations of FET based SCRs and caution the circuit designers about using SCRs in the place of conventional resistors.

**Keywords:** Switched capacitors resistors, parasites in SCR, FET, MOSFET, EMOSFET.

### I. INTRODUCTION

The principles of operation of ideal SCRs and, the extent to which SCRs can be represented by a conventional resistor are described. The effect of switch resistance on the value of SCR and the attempts to compute the SCR values taking the I-V characteristics of the switches are discussed. The behavior of SCR [1] when connected along with conventional capacitors and resistors are considered. We caution on the use of SCRs in the place of conventional resistances as they mimic the behavior of conventional resistors only under some special circumstances. Switched capacitor circuits are based on the principle that “charge transfers from a higher voltage node to a lower voltage node”. This is generally carried out in two steps, charging a capacitor to a voltage  $V_1$  through a switch and discharging it to a lower voltage  $V_2$ , through another switch.

Under equilibrium conditions the charge drawn from the high voltage node is the same as the charge delivered to the low voltage node. This charge transfer takes place [2] in one clock period and the average rate of charge transfer is taken as the DC current, even though the current is impulsive (for ideal conditions). The ratio of voltage difference to the current is taken as the effective resistance of the SCR. Switched Capacitor acts like a resistor whose value depends on capacitance  $C_s$  and switching frequency  $f$ . The switched capacitor resistor is used in place of simple resistors in integrated circuits. Many configurations are suggested, and two of these are given.

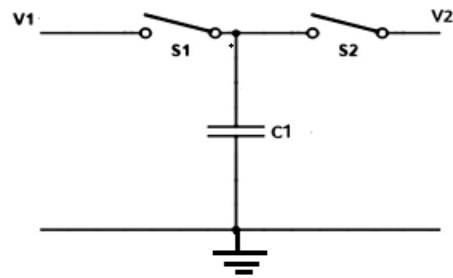


Fig. 1. Switched capacitor.

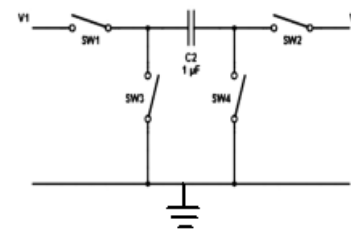
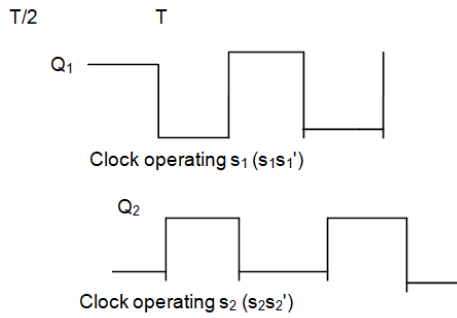


Fig. 2 (a) Configuration of switched- capacitor.

The switched capacitor is shown in Fig.1 and its configuration is shown in Fig. 2.  $S_1$  and  $S_2$  are the switches as in Fig. 1 and ( $S_1, S_1'$ ) and ( $S_2, S_2'$ ) are operated by non-overlapping clocks as shown in Fig. (2b). Switches close when  $Q$  is high and open when  $Q$  is low where  $Q$  is the control voltage.



**Fig. 2 (b)** Operating clocks.

The average value of current flowing from  $V_1$  to  $V_2$  is average value  $I = \frac{C(V_1 - V_2)}{T}$  (1)

and the effective resistance is given by

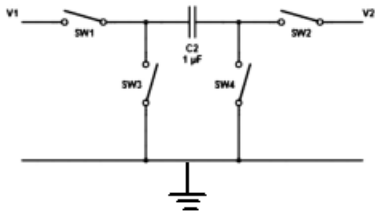
$$R = \frac{T}{C} \left( \frac{V_1 - V_2}{I} \right) \quad (2)$$

$$= T/C = 1/Fc \text{ (iii), where } f = 1/T \quad (3)$$

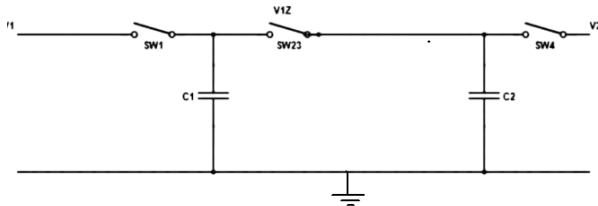
It may be seen from this description that SCR is a variable resistor whose value can be varied by varying the switching frequency. If this SCR is to be used to replace conventional resistors, [9] it is necessary to know to what extent this SCR resembles a conventional resistor.

## II. SERIES CONNECTED SCRs

**Case 1.** Let two SCRs are operated by the same non-overlapping clocks are connected in series as shown in Fig. 3.



**Fig. 3 (a)** SCR's connected in series.



**Fig. 3 (b)** SCR's connected in series.

If we follow the sequence of operations for both the resistors as described for SCR in Fig. 1, we realize that  $S_1$  and  $S_3$ ,  $S_2$  and  $S_4$  are to be synchronously operated [8] in which either  $S_2$  or  $S_3$  is always open and hence no charge transfer can take place between  $V_1$  and  $V_4$ . This clearly indicates that SCRs cannot be connected with the same sequence of operations for realizing the combined effect. To understand the impact of the series connection of resistors follow the logic that charge is to be transferred from node  $V_1$  to node  $V_{23}$  and then to node  $V_4$ . In other words, the charge is transferred in steps (i.e.) from  $V_1$  to  $C_1$  from  $C_1$  to  $C_2$  and then  $C_2$  to  $V_2$ . This can be achieved by synchronously

operating  $S_1$  and  $S_4$  and  $S_2$  and  $S_3$ . A single switch  $S_2$  can replace  $S_2$  and  $S_3$  and the operation is described as follows.

— Close  $S_1$ ,  $S_4$  and open  $S_{23}$ .  $C_1$  is charged to  $V_1$  and  $C_2$  is discharged [12] to  $V_2$ .

— Then open  $S_1$ ,  $S_4$  and close  $S_{23}$ . Then some charge gets transferred from  $C_1$  to  $C_2$  and the voltage  $V_{23}$  is given by

$$V_{23} = \frac{C_1 V_1 + C_2 V_2}{C_1 + C_2} \quad (4)$$

(both  $C_1$  and  $C_2$  have this voltage)

— When step 1 is repeated charge is transferred from  $V_1$  to  $C_1$  and from  $C_2$  to  $V_2$ . The charge transferred is  $Q = C_1(V_1 - V_{23}) = C_2(V_{23} - V_2)$  (5)

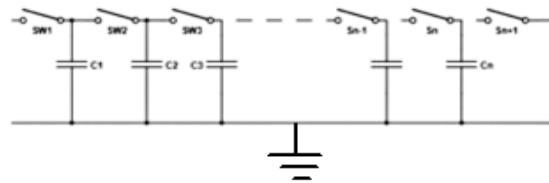
Substituting for  $V_{23}$  from (4.2.1) in (5.2)

$$Q = \frac{C_1 C_2 (V_1 - V_2)}{C_1 + C_2} \quad (6)$$

$$\text{The average current flowing} = I = \frac{C_1 C_2 (V_1 - V_2)}{T \cdot (C_1 + C_2)} \quad (7)$$

$$\text{Effective resistance} = \frac{T}{C_1} + \frac{T}{C_2} = R_1 + R_2 \quad (8)$$

We can connect several SCRs in services as shown below. The sequence of operations to be followed is that alternate switches have to be synchronously operated by a non-overlapping clock



**Fig. 4.** SCRs in series.

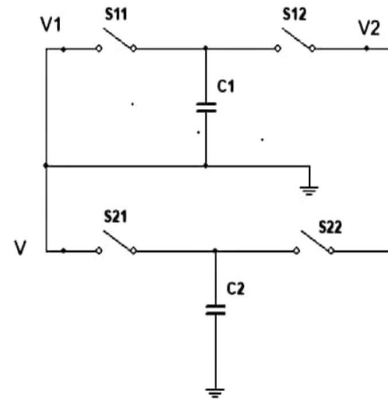
$$\text{Equivalent resistance} = R_1 + R_2 + R_m - R_n \quad (9)$$

$$\text{where } R_m = \frac{T}{C_m} = \frac{1}{f \cdot C_m} \quad (10)$$

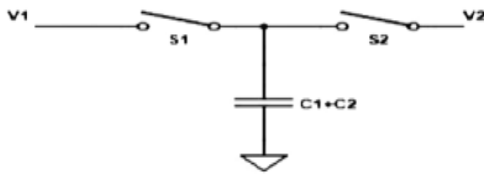
This analysis shows that SCRs connected in series with the switching sequence described above behave like a stack of normal resistances [13] connected in series.

## III. PARALLEL CONNECTED SCRs

SCRs may be connected in parallel as shown in the Figs. 5, 6.



**Fig. 5.** SCRs in parallel.



**Fig. 6.** SCR s in parallel.

From the figure, it is clear that there is no change in the sequence required and the overall resistance is

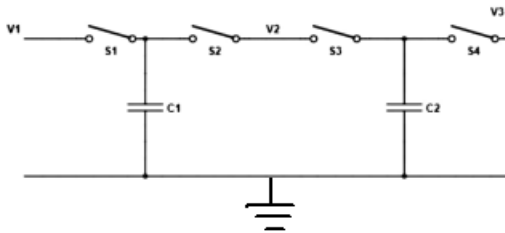
$$R = \frac{T}{C_1 + C_2} \quad (11)$$

$$G = \frac{C_1 + C_2}{T} = \frac{C_1}{T} + \frac{C_2}{T} = G_1 + G_2 \quad (12)$$

SCRs when connected in parallel, they behave like parallel stack of conventional resistors.

#### IV. SCR WITH DIFFERENT OPERATING SWITCHING FREQUENCIES

In the first in stage, let there be two switches for each resistor and they are operated normally.



**Fig. 7.** SCRs in different operating frequencies.

Except that the clock is shifted from the other by a certain time 'S'. This shift enables  $S_2$  and  $S_3$  closed deriving 'S'. If 'S' is sufficient for the charge to get redistributed between  $C_1$  and  $C_2$ , the resistors follow the law of addition (i.e.  $R = R_1 + R_2$ ).

Let the switching frequency of one resistor [18] be double the switching frequency of the other but synchronized. In this situation the charge gets transferred from  $V_1$  to  $V_2$  only, at the rate decided by the lower switching frequency. This leads to the discrepancy in the effective resistance value. Normally the effective resistance should be  $R = R_1 + R_2 = \frac{T_1}{C_1} + \frac{T_1}{2C_2}$ .

However, in this case it would be

$$\frac{T_1}{C_1} + \frac{T_1}{2C_2} \quad (13)$$

Thus whenever resistors realized with different [20] frequencies are connected in series, the effective value of the stack is decided by the lower switching frequency.

##### A. Parallel connected SCRs

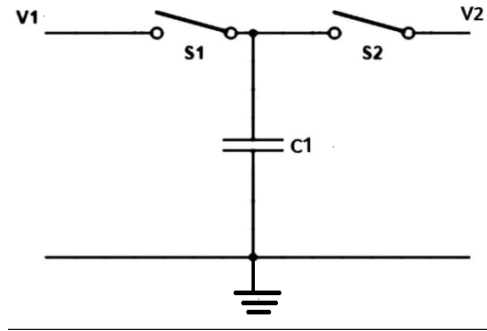
Since each branch of the parallel stack [6] generates an average current independent of other branch, the sum of all the average currents would be the effective average current and hence the parallel resistor property is still valid even if the switching frequencies of operation are different.

Thus it may be mentioned that SCRs operating with different switching frequencies when connected in series, the effective value does not follow the normal rule of series-connected to conventional resistors follow whereas parallel SCR stack obeys the normal rules followed by conventional resistors.

##### B. Power dissipation in SCRs

One may wonder whether there is any power dissipation in SCRs as there is no visible dissipative element as it contains only capacitors and ideal switches. But there is hidden power dissipation in the form of switching losses. It is known that while a capacitor is charged to a voltage  $V_1$ , there is a loss of energy equal to  $\frac{1}{2} CV^2$  and the stored energy is only  $\frac{1}{2} CV^2$  (i.e.) the efficiency of charging is only 50%. When the capacitor discharges, there is energy loss. In this section, the energy losses and hence the power loss [22] in SCR because of switching is calculated.

##### C. Energy loss calculations



**Fig. 8.** Switched capacitor.

Step 1: Energy stored (extra) when the capacitor is charged from  $V_2$  to  $V_1$ .

$$V_1 = \frac{1}{2} C (V_1^2 - V_2^2) \quad (13a)$$

Energy drawn from  $V_1$  to store this energy

$$E_{V_1} = v_1 \int_{V_2}^{V_1} C dv = C (V_1^2 - V_1 V_2) \quad (14)$$

Energy dissipated during charging

$$C (V_1^2 - V_1 V_2) - \frac{1}{2} C (V_1^2 - V_2^2) \quad (15)$$

$$E_{d_1} = \frac{1}{2} C (V_1 - V_2)^2 \quad (16)$$

Similarly the charge dissipated during discharging from  $V_1$  to  $V_2$  can be shown to be

$$E_{d_2} = \frac{1}{2} C (V_1 - V_2)^2 \quad (17)$$

Total energy dissipated 'E' during one cycle (i.e.) in a period T is given by

$$\text{Energy dissipated } E = C (V_1 - V_2)^2 \quad (18)$$

$$\text{Power dissipated } = P = \frac{C (V_1 - V_2)^2}{T} = (V_1 - V_2)^2 / (T/C) \quad (19)$$

Thus, the energy dissipated in SCR operating between  $V_1$  and  $V_2$  or with voltage difference of  $(V_1 - V_2)$  is the same as that takes place in the case of a conventional resistor operating under the same conditions.

$$\frac{(V_1 - V_2)^2}{R} \quad (20)$$

From the above analysis we may conclude that the [4] SCR under ideal situations can mimic the behaviour of a resistor from the point of series and parallel connected resistors and power dissipation. However when the resistors are realized with different switching frequencies and if they are connected in series [16], the effective [3] resistance is controlled by lowering the switching frequencies. .

##### D. Behaviour of SCR when connected to normal components

From the circuit given above, it may be seen that during charging [5] from  $V_1$  the current is impulsive and while discharging the current varies exponentially with time and the voltage  $V_{R_L}$  and I can be obtained as

$$VR_L = V_1 e^{\frac{-T}{2R_L C}} \quad (21)$$

and the average current

$$I = \frac{C(V_1 - V_1 e^{\frac{-T}{2R_L C}})}{T} \quad (22)$$

The equivalent resistance  $R_{eq}$  is given by

$$R_{eq} = \frac{T}{C(1 - e^{\frac{-T}{2R_L C}})} \quad (23)$$

This value is different from the expected value of  $R_{eq} = \frac{T}{C} + R_L$  (24)

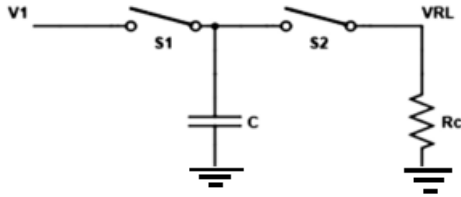


Fig. 9. SCR connected to normal components.

Thus, when SCR is connected with [14] conventional resistor in series. One should be very careful in computing the effective resistance. However, when connected in parallel, the conductance can be calculated using the normal rules.

### V. SCRs WITH PRACTICAL SWITCHES

When SCRs are realized with electromechanical switches, which have almost ideal characteristics “on resistance is very close to zero and off resistance is very high”. The SCRs are expected [7] to behave like ideal SCRs. However, when they are realized with switches like BJT or FET switches, SCR behaviour is expected to change. The following investigations are carried out on SCR with EMOSFET switches.

#### A. EMOSFET as a switch

“On and off” states (between same and drain) are controlled by the gate to source voltage ( $V_{gs}$ ). The following may be kept in mind while realizing SCRs with FETs.

- FET conducts reasonably well when  $V_{gs} > V_T$
- There is a voltage [8] drop  $V_{DS}$  depending on the current  $I_D$  or  $I_S$  which gives rise to resistance.
- There is a channel charge stored under the gate when conducting and it has to be discharged in the off conditions.
- There are FET capacitances like  $C_{Ds}$  and  $C_{Gs}$

#### B. Charging of a capacitor using FET

In SCR, the charging and discharging are carried out using FETs and the FETs go through varying currents and voltages ( $V_{gs}$  and  $V_{DS}$ ) with time. Thus, the resistance offered is a variable resistance with time. This results in a gradual variation of current while charging [15] or discharging unlike in the case of ideal switches. In view of this charging and discharging process in SCR, the I-V relation of FETs are calculated and the equivalent resistance is obtained.

#### C. SCR analysis using FET switches using I-V relation

Consider the following circuit for SCR

Under equilibrium conditions let the capacitor C gets charged from  $V_1$  to  $V_c$  while charging and let it get discharged from  $V_c$  to  $V_D$  during the discharging period.

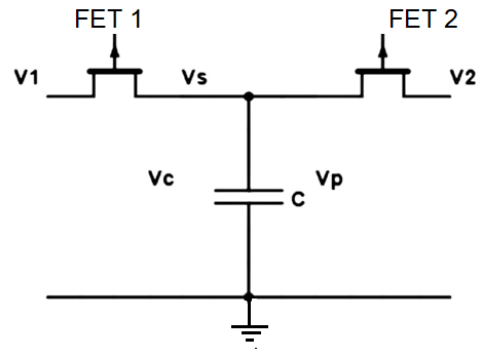


Fig. 10. SCR using FET.

The I-V relation used for MOSFET<sub>1</sub> is

$$I_o = I_{DSS} [(V_G - V_S - V_T)(V_1 - V_S) - 1/2(V_1 - V_S)^2] \quad (25)$$

The voltage  $V_s$  charges with time and is given by

$$\frac{dV_s}{dt} = \frac{I}{C} \quad (26)$$

using the equations 25 and 26 and with the boundary conditions  $V_s = V_D$  at  $t = 0$  and  $V_s = V_c$  at  $t = T/2$   $V_c$  is shown as below.

$$V_c = V_1 - \left[ \frac{2b}{e^{-\frac{I_{DSS} b T}{2C}} \left(1 + \frac{2b}{V_1 - V_D}\right) - 1} \right] \quad (27)$$

Where  $b = (V_g - V_T - V_T)$  (28)

During discharge, the  $V_{gs}$  remain constant and  $V_{DS}$  changes. We can show that

$$V_d = V_2 + \frac{2a}{1 + \left(\frac{2a}{(V_c - V_2)} - 1\right) e^{\frac{I_{DSS} a T}{2C}}} \quad (29)$$

#### D. Evaluation of SCR resistance taking the I-V characteristics of FET switches

Consider Fig. 10. The charging and discharging controlled by [7] FET switches, taken place following the I-V characteristics of the FETs. The equation describing I-V relation of FET is taken as

$$I_D = I_S = I_{DSS} [(V_{GS} - V_T)V_{DS} - 1/2 V_{DS}^2] \quad (30)$$

When FET 1 is put on with a gate voltage  $V_g$  and FET 2 is put off. Then the capacitor [8] gets charged from a voltage  $V_D$  to  $V_c$  from the source  $V_1$  where,  $V_D$  is the voltage at  $t = 0$  across the capacitor and [22]  $V_c$  is the voltage at  $t = T/2$ ,  $V_c$  [19] and  $V_D$  are the equilibrium or steady state values.

It may be noted that during charging, the capacitor voltage [10] which is the source voltage continuously changes with time. The variation source voltage may be obtained by

$$\frac{dV_s}{dt} = \frac{I}{C} \quad (31)$$

$$I = I_{DSS} [(V_G - V_S - V_T)(V_1 - V_S) - \frac{1}{2}(V_1 - V_S)^2] \quad (32)$$

The above equation may be written as given below.

$$I = I_{DSS} [(V_g - V_1) + (V_1 - V_S) - V_T] (V_1 - V_S) - \frac{1}{2} (V_1 - V_S)^2 \quad (33)$$

$$\text{Det } V_1 - V_S = X \text{ and} \quad (33a)$$

$$V_g - V_1 - V_T = B \quad (33b)$$

$$\text{Then } I = I_{DSS} [(b+x) - \frac{1}{2}X] X \quad (34)$$

From (30) and (33)

$$\frac{dV_s}{dt} = \frac{dx}{dt} = \frac{I}{C} = \frac{I_{DSS}}{C} [(b+x)x - \frac{1}{2}x^2] \quad (35)$$

Integrate this Eqn. (8) with respect to time realizing

$$\text{At } t = 0, x = V_1 - V_D \text{ and} \quad (36)$$

$$T = T/2. X = V_1 - V_C \quad (37)$$

We obtain

$$V_c = V_1 - \frac{2b}{\frac{me}{IdssbT} - 1} \quad (38)$$

Where  $m = \frac{2b-v_1-v_d}{v_1-v_d} \quad (39)$

$$b = V_g - V_1 - V_T \quad (40)$$

During discharging of the capacitor, FET1 is off and FET2 is on. The capacitor discharges from  $V_c$  (at  $t = 0$  beginning of discharging) to  $V_d$  (at  $T = T/2$  end of discharging). Further it may [11] be noted that  $V_s$  remains constant at  $V_2$  and  $V_D$  changes with time.

The current flowing through FET during this period is given by

$$I = Idss [(V_g - V_2 - V_T) (V_D - V_2) - 1/2(V_D - V_2)^2] \quad (41)$$

Further,

$$dV_D/dt = -I/C \quad (42)$$

Also let  $V_D - V_2 = y$ ,

$$dV_D / dt = dy/dt \quad (47)$$

$$V_g - V_2 - V_T = a$$

$$\text{Then } \frac{dy}{dt} = \frac{-Idss}{2C} (2a-y)y \quad (48)$$

Integrating this equation w.r.t  $y$  and using the boundary conditions

$$Y = V_c - V_2 \text{ at } t = 0 \quad (49)$$

$$Y = V_d - V_2 \text{ at } t = T/2 \quad (50)$$

Then

$$V_d = V_2 + \frac{2a}{\frac{1+ne}{IdssaT} - 1} \quad (51)$$

$$n = \frac{2a - V_c + V_2}{V_c - V_2} \quad (52)$$

$$a = V_g - V_2 - V_T \quad (53)$$

Table 1.

Tnsec	Vc(V)	Vd(V)	C	V1	V2	Res of SCR
16	1.996	1.921	2pF	2.0	1.0	53 kΩ
30	1.999	1.910	2pF	2.0	1.0	84.34 kΩ

If we examine equations from (33) to (42) we find that they contain  $V_c$  and  $V_d$  and they are related by these equations. For a given  $V_1$  and  $V_2$  and for specific values of  $T$ ,  $C$ , and  $I_{DSS}$  one can solve for  $V_c$  and  $V_d$  using a method like graphical method. In this paper, graphical method is used and typical values of  $V_c$  and  $V_d$  are given in table for different values of  $T$ .

The average current is  $(V_c - V_d)C / T \quad (43)$

and the resistance is  $(V_1 - V_2) / (V_c - V_d) \cdot T / C \quad (44)$

the equations 41 and 42 are simultaneously solved for  $V_c$  and  $V_d$  (using a graphical method) for a set of  $V_1$  and  $V_2$  and FET knowing the value of  $V_c$  and  $V_d$ , the total charge transferred in a cycle is

$Q = C(V_c - V_d)$  and the average current is

$$I = \frac{Q}{T} = \frac{C(v_c - v_d)}{T} \quad (45)$$

is calculated and hence the resistance  $R$  as

$$R = \frac{V_1 - V_2}{I} = \frac{(V_1 - V_2)}{(v_c - v_d)} \left( \frac{1}{C} \right) \quad (46)$$

This shows that for a given  $V_1 > V_2$  the value of resistance increases by a factor  $1/V_c - V_d$  for a time period of 30n sec and

$I_{DSS} = V_g V_1$ ,  $V_2$  are calculated.

The expected resistance has gone up by a factor of 5 times. (84 kΩ instead of 15kΩ).

The SCR [23] is simulated and the resistance is measured and it is about twice the ideal value.

From this it is clear that the switch resistance increases the effective value by as much as 2-5 times that of ideal resistance values since the actual value (measured value) is far from that of ideal SCR and the calculated value, and also it is too complicated to calculate the SCR value taking the I-V characteristics into account, The charging characteristics of the capacitor with FET is measured as shown in Fig. 11.

$V_g = 2V$

The variation of  $V_0$  with time is noted, the time needed for  $V_0$  to reach about 65%  $V_D(2V)$  is noted then the equivalent resistance of FET to charge the capacitor in the same time period is calculated (i.e.) FET may be replaced by this resistor for charging and discharging purpose.

SCR with FET represented (modelled) by  $R_{eq}$  (described above)

The charging and discharging characteristics with equivalent resistor present in SCR are calculated and the  $V_c$  and  $V_d$  (as defined in the earlier case are shown.

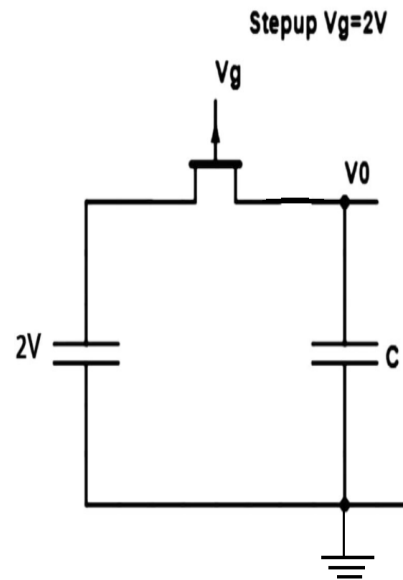


Fig. 11. Circuit diagram of FET.

E. Evaluation of SCR resistance with FET represented by a constant equivalent resistor, using the same notation as in (D)

Replacing the FETs by their "On resistances" when they are closed and by  $\infty$  resistance when they are open the values of  $V_c$  and  $V_d$  are calculated using the following procedure. The SCR equivalent circuit may be sketched as shown in the Fig. 11.

During charging 'C' gets charged from  $V_d$  to  $V_c$  from voltage  $V_1$  and during discharging its gets [17] (c) discharged from  $V_c$  to  $V_d$  into  $V_2$ . The current  $I$  following into  $C$  during charging is

$$I = C \frac{dv}{dt} = \frac{V_1 - V}{R} \quad (54)$$

This equation may be solved for  $V$  with the boundary condition that  $V = V_d$  at  $t = 0$  and  $V = V_c$  at  $t = T/2$ .

This resulting in  $V_c = V_1 + (V_d - V_1) e^{-\frac{T}{2RC}}$  (55)

Similarly the value of  $V_d$  can be shown to be  $V_d = V_2 + (V_C - V_2) e^{-\frac{T}{2RC}}$  (56)

The average current is given by

$$I_{av} = \frac{V_C - V_d}{T} C \quad (57)$$

The resistance of SCR is given by  $R = \frac{(V_1 - V_2)}{(V_C - V_d)} \left(\frac{T}{C}\right)$  (58)

using different values of 'R' corresponding to different operating ranges resistance value of SCR are calculated and it is found that value of R corresponding to about 70% charging of the capacitor with FET gives reasonable value of SCR.

$$V_C = V_1 + (V_d - V_1) e^{-\frac{T}{2RC}} \quad (59)$$

$$V_d = V_2 + (V_C - V_2) e^{-\frac{T}{2RC}} \quad (60)$$

These two equations are solved for  $V_D$  and  $V_C$  for a given  $V_1$  and  $V_2$ . Then the average current is calculated as

$$C(V_C - V_D)/T \quad (61)$$

and the resistance as

$$R = \frac{(V_1 - V_2)}{(V_C - V_d)} \left(\frac{T}{C}\right) \quad (62)$$

The calculated value for a time period of 30ns is about 17k $\Omega$ . The ideal value is 15k $\Omega$ . However, the corresponding measured value of SCR is 32.89 K $\Omega$ . This corresponds to the equivalent resistor corresponding to 70% of  $V_D$ .

## VI. CONCLUSION

From this analysis, it is clear that the SCR resistance with FETs is generally higher than ideal resistance. If FET is replaced by an equivalent resistor corresponding to that of 65% value (refers charging of capacitor with FET). The SCR value would be the same as that of ideal one. However, the measured resistance of SCR with FETs is higher than that of ideal one by a factor of 2, where SCR is replaced by resistor of value equal to the equivalent resistor needed for charging the capacitor to 65% of the peak value in the slew time.

In addition to the above investigation, resistance of SCR with FETs switches is measured with a small capacitance connected between source and drain of the FETs. It is found that the effect of the capacitor on SCR resistance value is not significant as long as this capacitance is small compared to the main capacitor. Similarly the effect of leakage of the switching capacitor is found to be negligible as long as the leakage current is small compared to the average current. The following observations are mentioned.

- SCR with ideal switches can mimic the behaviour of conventional resistor from the point of connecting SCR in series, in parallel and from the point of power dissipation.

- SCR with MOSFET switches exhibits resistance values and the FET parameters if it is connected. In a typical case the effective resistance is approximately the value of ideal SCR with the same switching frequency and the charging capacitor.

- SCRs when connected in series, operating with different frequencies, the value of the effective resistance is decided by the lower switching frequency.

- When SCRs are connected in parallel the effective resistance follows the rule applicable to conventional resistors and the operating frequencies.

- When SCRs are loaded with resistive loads the effective resistance is not same as the sum of the resistors values.

- Even with capacitive loads, the output wave forms obtained with the SCRs is different from those obtained with the conventional resistors by the same value.

- SCRs can take small parasitic capacitances across the switches.

In the end we may caution on the use of SCRs in the place of conventional resistances as they mimic the behavior of conventional resistors only under some special circumstances. However, one can evaluate the performance of the circuits using SCRs, taking the actual charging and discharging characteristics of the capacitor through the equivalent resistance of the FET switches.

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## REFERENCES

- [1]. Soclof, S. (1991). *Design and applications of analog integrated circuits*. Prentice Hall.
- [2]. Allen, P. E., & Holberg, D. R. (2011). *CMOS analog circuit design*. Elsevier.
- [3]. Zhu-ping, W., Shun-an, Z., Xiao-qing, W., & Dan-dan, N. (2010). Design of a high-precision low-pass switched-capacitor filter. In *2010 International Conference on Electrical and Control Engineering*, 707-709. IEEE.
- [4]. Baker, R. J. (2019). *CMOS: Circuit design, layout, and simulation*. John Wiley & Sons.
- [5]. Behzad Razalli (2007). *Design of analog CMOS integrated circuits*, Chapter 12 introduction to switched capacitor circuits, Tata MC-Grawhill, New Delhi .
- [6]. Kimball, J. W., & Krein, P.T. (2005). *Analysis and design of switched capacitor converters*, 1473–1477.
- [7]. Baschiroto, A. (2001). Low-voltage switched-capacitor filters. *Proceedings 2001 19th NORCHIP Conference. Technoconsult*, Copenhagen, Denmark, 10-20
- [8]. Baker, R. J., Harry, W. Li, David & Boyce, E. (2000). CMOS circuit design, layout and simulation Chapter 27", *Dynamic analog circuits IEEE Press, Prentice Hall of India Pvt. Ltd., New Delhi*.
- [9]. Winder, S. (2000). *Analog and Digital Filter Design. Elsevier Science (USA)*.
- [10]. Grise, W. R. (1999). Applications of switched-capacitor circuits in active filters and instrumentation amplifiers. *Technology Interface*, 3(3),
- [11]. Joardar, K., Gullapalli, K. K., McAndrew, C. C., Burnham, M. E., & Wild, A. (1998). An improved MOSFET model for circuit simulation. *IEEE Transactions on Electron Devices*, 45(1), 134-148.

- [12]. Johns, D. A., & Martin, K. (1997). *Analog integrated circuit design*. Chapter 10 -switched capacitor circuits P John Wiley & Sons Inc.
- [13]. Schrom, G., Stach, A., & Selberherr, S. (1996). A consistent dynamic MOSFET model for low-voltage applications. In *1996 International Conference on Simulation of Semiconductor Processes and Devices. SISPAD'96 (IEEE Cat. No. 96TH8095)*, 177-178. IEEE.
- [14]. Chandrakasan, A. P., & Sheng, S. (1995). RW Brodersen, Low Power Digital CMOS Design.
- [15]. Wereley, N. M., & Hall, S. R. (1990). Frequency response of linear time periodic systems. In *29th IEEE conference on decision and control*, 3650-3655. IEEE.
- [16]. Mohan, N., & Patil, R. L. (1987). Active filter without using external capacitors. *Journal of instrumentation society of India*, 7(2), 212-216.
- [17]. Sandler, H. M., & Sedra, A. S. (1986). Programmable switched-capacitor low-pass ladder filters. *IEEE journal of solid-state circuits*, 21(6), 1109-1119.
- [18]. Allen, P. E., & Sinencio, E. S. (1984). Switched Capacitor Circuits", *Van Nostrand Reinhold, New York*.
- [19]. Mohan, P. A., Ramachandran, V., & Swamy, M. N. S. (1984). New general biquadratic active RC and switched-capacitor filters. In *IEE Proceedings G-Electronic Circuits and Systems*, 131(2), 51-55.
- [20]. Fischer, J. H. (1982). Noise sources and calculation techniques for switched capacitor filters. *IEEE Journal of Solid-State Circuits*, 17(4), 742-752.
- [21]. Temes, G. C. (1980). Finite amplifier gain and bandwidth effects in switched-capacitor filters. *IEEE Journal of Solid-State Circuits*, 15(3), 358-361.
- [22]. Bandyopadhyay, A. K. (1980). Equivalent circuit of a switched capacitor simulated resistor. *Proceedings of the IEEE*, 68(1), 178-179.
- [23]. Kurth, C., & Moschytz, G. (1979). Nodal analysis of switched-capacitor networks. *IEEE Transactions on Circuits and Systems*, 26(2), 93-105.

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