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Designing and Implementation of Arduino based Laboratory PMU

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ABSTRACT: Phasor Measurement Unit (PMU) uses synchro-phasor technology to give time stamped voltage, current phasor at higher reporting rate than that of Supervisory Control and Data Acquisition(SCADA) in both transmission and distribution networks. Phasor Measurement Unit (PMU) is one of the technologies of Wide Area Measurement System which provide information for analysis and protection of power system. The main purpose of the paper is to design laboratory prototype of Phasor Measurement Unit (PMU) which gives voltage and current measurements across resistive load at residential level of power grid in real time. The laboratory prototype of PMU consists of anti-aliasing filter, phase locked oscillator, Current Transformer, Potential Transformer and Arduino Mega. In the proposed work, modelling of anti-aliasing filter and phase locked oscillator are done. Thereafter, Discrete Fourier Transform phase estimation technique at sampling rate of 80 kHz is used to process the voltage signal taken across resistive load at residential level of power grid in real time. The designed PMU gives voltage magnitude and phase, voltage magnitude and phase corresponding to current signal at the same time in compliance with IEEE standard C-37.118(2011). As there is seldom work done on a laboratory prototype of PMU, so there was very less literature for the same. The present work in this research area includes optimum placement of PMU in micro-grid systems and distribution systems. This paper demonstrates a laboratory prototype of PMU which can be useful for academic demonstration as well as for research purpose.

Keywords: SCADA, PMU, GPS, DFT, Anti-aliasing filter, Phase locked oscillator, Pulse generator.

I. INTRODUCTION

There have been significant grid unsettling influences on the 30th and the 31st July 2012 which have influenced huge pieces of the Indian Electricity Grids. Because of high burden and disappointment of storm, Northern Region was drawing a huge quantum of intensity from neighbouring Western and Eastern Grids while because of downpours in Western Region request was less and it was under drawing. This circumstance prompted a much slanted burden age balance among the districts. A large quantum of intensity was spilling out of the Western Grid toward the Northern Grid straightforwardly just as through the Eastern Grid and the framework was under pressure [1-4].

On August 14, 2003, North America suffered its biggest power outage. Major 345 kV transmission lines dropped out of administration, unbeknownst to administrators, causing a falling blackout that reached out over the Midwest, Northeast, and into Canada [1]. An examination propelled by the North American Electric Reliability Corporation (NERC) found that the power outage could have been confined to a little district had administrators known the status of overstressed and falling lines [5-7].

The load dispatch focuses in a huge power framework direct and command over the transmission Network and it takes preventive activities to maintain a strategic distance from any kind of framework disappointment which can hamper power dispersion. With consistently expanding size and unpredictability of the power framework, the capacity to recognize any flaws in the power framework is intensely reliant on the ongoing data accessible to the administrator. Generally, simple and advanced data (status of electrical switch, control stream and recurrence) is estimated at the substation level and transmitted to stack dispatch focus utilizing supervisory control and information obtaining framework (SCADA) or vitality the board framework (EMS). The significant constraint of SCADA or EMS is the powerlessness to precisely figure the stage edge yield between a couple of substations. In SCADA or EMS, stage point is either evaluated from accessible information or is determined disconnected. Phasor Measurement Units (PMU) beats the restrictions of SCADA and EMS by precisely ascertaining the stage edge between a couple of matrix [8-10].

Synchronized phasor estimation units were exhibited in the mid-1980s as a response for the need of continuously capable and progressively secure watching devices for Electric Power Systems (EPS). Starting now and into the foreseeable future, evaluating Electric Power System (EPS) parameters of voltage and energy for the most part far away transports has gotten phenomenal thought from researchers. Such estimations are performed by phasor estimation units (PMUs), synchronized by Global Positioning System (GPS) satellites [11].

The PMUs are estimation gadgets intended to gauge phasor, frequency and pace of progress of frequency (ROCOF) of electrical sign, for example, voltages and flows in control systems, utilizing a wellspring of time

synchronization to label every estimation with the comparing moment. The synchronized idea of the PMU estimations requires the presentation, under another point of view, of old style ideas, for example, the phasor. Such estimations are performed by phasor estimation units (PMUs), synchronized by Global Positioning System (GPS) satellites [12].

The synchro-phasor is actually dedicated to interface the phasor idea to its estimation in an unambiguous manner. Actually, the synchro-phasor estimation depends on a similar thought fundamental the phasor, with the primary contrast that the phasor and, specifically, its stage edge, is determined utilizing Coordinated Universal Time (UTC) as a period reference. Such decision permits having a one of a kind reference for all the sinusoidal sign to be estimated in a wide or worldwide zone, on the grounds that the time dispersal depends on satellite frameworks. Two synchro-phasors, determined at various focuses in a system, can be effectively contrasted in light of the fact that they are connected with basic moments [6, 9].

The amplitude based on total vector error, phase angle scan and dynamic test is carried on the DTU-PMU and the PMU-1 is carried out before the IEEE standard modulation testing [13]. A MATLAB based front end graphical user interface (GUI) is developed to acquire the information of peak values, power and phase angles, from the PMUs using a centralized Intelligent Electronic Device with time synchronized pulses in multicast mode [14]. A Synchronised Phasor Measurement Unit (PMU) based on Recursive Discrete Fourier Transform (DFT) algorithm is simulated in LabVIEW software in reference to a signal from global positioning system [15]. A PMU prototype based on a Field Programmable Gate Array (FPGA) is designed iterative-Interpolated DFT (i-IpDFT) and evaluated in terms of the latency [16].

As the power system is growing day by day there is an essential need of reliable and efficient devices which can monitor phase angles of both voltage and current and rate of change of frequency. Various PMUs are as of now introduced in a few utilities around the globe for different applications, for example, post mortem applications, adaptive protection scheme, and state estimation. But in available literature lesser work is done on laboratory prototype of PMU, thus main focus of the proposed work is to design and develop such prototype for research purpose. In the paper 4th order Butterworth low pass filter is used as anti-aliasing filter to obtain fundamental frequency component. Modelling of phase locked oscillator is also done to generate sampling pulses at higher frequency and then hardware implementation of anti-aliasing filter and phase locked oscillator is discussed in the paper. The paper also describe phasor estimation technique to obtain voltage phasor of signal taken from 230 V, 50 Hz AC source across which a resistive load is connected in compliance with IEEE standard C37.118.1 [8]. Then integration of different units to design laboratory PMU and its testing in real time are presented in the paper. The present work in this area includes development of PMU for distribution networks and micro-grid. These use synchro-phasor processor which receives 1 PPS signal from GPS located at PMU location. In the proposed work, Laboratory prototype is developed compared to the already present distribution networks PMU. The proposed work can be implemented for research purposes.

The design and development of PMU Laboratory prototype is carried out in the paper. The recent works in this area does not include any development of PMU for a laboratory type as there have been works on PMU on distribution networks and micro-grids. Advantages of the proposed work includes a laboratory purpose of PMU which can be useful for demonstration of basic working of PMU and research purposes for its further development.

II. IMPLICATIONS OF EXISTING METHODS

Present technology of phasor measurement units is highly advanced. When this technology was developed the prime focus of power utilities is to protect and stabilize transmission network as it is the backbone of the whole electrical grid system. At that time does not bother much about distribution system. But now the scenario is changed as the grids are becoming smart and consumers also demand's quality power. PMU do not function properly on the distribution system with current technology as problems in distribution system is far more complex than the problems present in the transmission system. Additional problems like unbalancing of system, harmonics etc. makes the current PMU technology incapable of solving the issues of distribution system. Also currently available PMU design is very bulky as it requires different units for data acquisition, communication and calculation of phase and magnitude of voltage and current. This makes the PMU costly and bulky. All these issues leads us to design a PMU which can used in distribution system along with transmission system and it does requires separate units for data acquisition, communication and calculation but is capable of doing all under one unit. This makes the PMU more affordable than current PMU'savailable in the market.

III. MATERIALS AND METHODS

DFT phasor estimation algorithm is based on steady state signal model. The voltage signal produced by the three-phase source in power transmission network at nominal frequency under steady state can be represented as:

$$v(t) = V_m cos(2\pi f_0 t + \varphi) \quad (1)$$

Where V_m is the peak amplitude of the signal, φ is the phase angle & f_0 is the on nominal fundamental frequency. Whenever the signal is sampled at the rate of N samples per cycle (sampling frequency Fs = Nf_0) then equation (1) becomes:

$$v(n) = V_m cos\,(2\pi n/N + \varphi) \quad (2)$$

Also, fundamental phasor of the given signal can be expressed as:

$$V = \frac{V_m}{\sqrt{2}} e^{j\varphi} \quad (3)$$

The N point DFT of the signal in (2) is [17]:

$$V(k) = \sum_{n=0}^{n=N-1} v(n) e^{-j2\pi k \frac{n}{N}} \quad (4)$$

Where k is the harmonic index whose value is taken as 1 to estimate the phasor of the fundamental frequency component. Therefore, the fundamental phasor of the

signal given in equation 3 estimated over a window of N samples, is given as:

$$V = \frac{\sqrt{2}}{N}\sum_{n=0}^{n=N-1} v(n)e^{-j2\pi\frac{n}{N}} \quad (5)$$

To update the phasor with each new input data sample acquired, the observation window is shifted by each sample.

The proposed laboratory PMU requires modelling of anti-aliasing filter, phase locked oscillator before their hardware implementation.

Simulation of anti-aliasing filter: The modelling of anti-aliasing filter is done in NI MULTISIM software as shown on Fig. 1. The circuit shown in Fig. 1 is Analog Butterworth low-pass filter. It is a cascade connection of two second order low pass circuit. The input is applied at pin number of Op-Amp 741 which is an AC signal of fundamental frequency of 50 Hz. The supply to the Op-Amp is provided at pin number 7 and grounded at pin number 4. The output from the first Op-Amp, taken from pin number 6 is fed as input to the second Op-Amp with the similar configuration as first part and the output is taken from pin number 6. The output is then observed on oscilloscope in software.

Simulation of phase-locked oscillator: The modelling of pulse generator which is used to generate required hundred pulse per second (PPS) taken by phase locked oscillator is shown Fig. 2.

The main component used in modelling is 555 timer IC which is an Astable multi-vibrator. The IC is powered from 6V dc source at pin number 4. Two feedback resistors are connected between 3 & 6 and 7 & 8 of values 1k ohm and 50k ohm respectively.

The modelling of the phase locked oscillator which is used to generate desired sampling pulses is done on PROTEUS software as shown in Fig. 3.

The circuit in Fig. 3 consists of PLL (Phase locked loop) IC 4046. The input is connected to potentiometer of 50k ohm value which is further connected to IC pin numbers 6 & 9. The input is a pulse signal of 100 Hz and the values of resistors and capacitors is according to the output frequency. The output is taken from pin number 4. The output is then observed on oscilloscope.

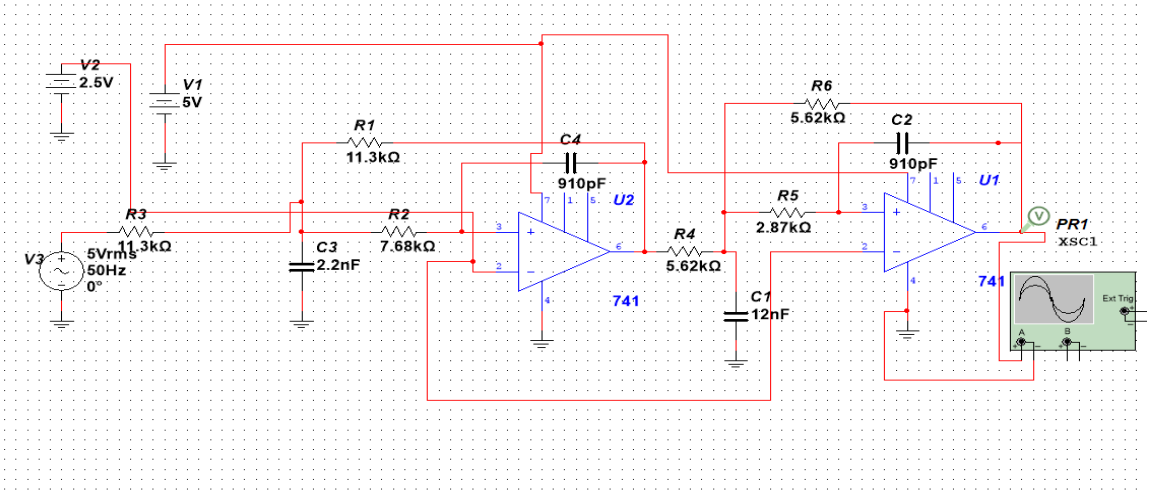

Fig. 1. Modelling of Anti-Aliasing filter.

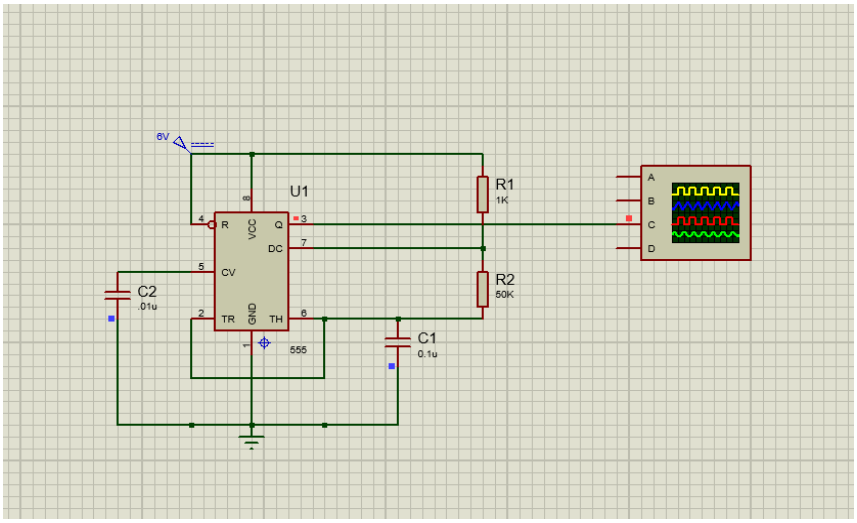

Fig. 2. Modelling of Pulse Generator.

Hardware Design: The step by step designing of laboratory PMU with separate designing of each unit is described in the following subsections:

Block Diagram: The block diagram of proposed laboratory PMU is demonstrated in Fig. 4.

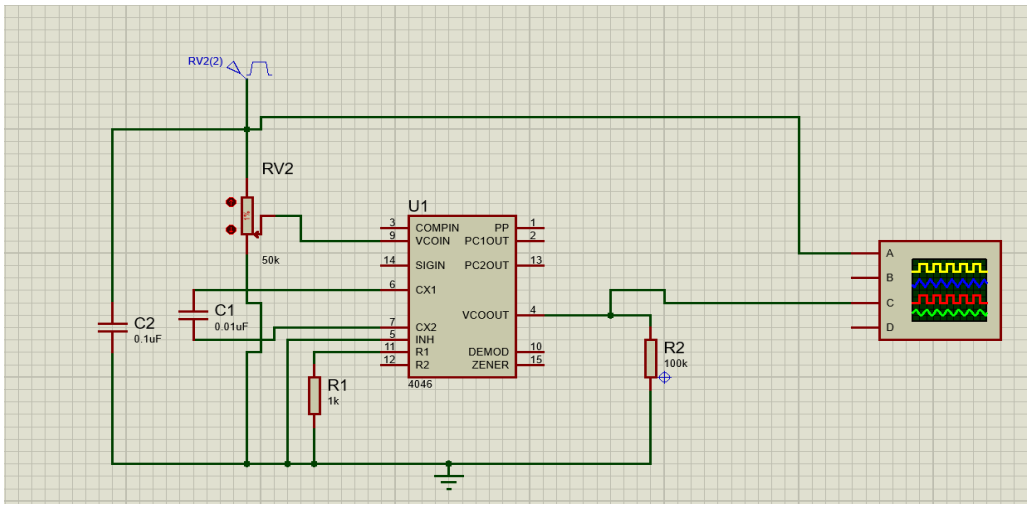

Fig. 3. Modelling of Phase-locked Oscillator.

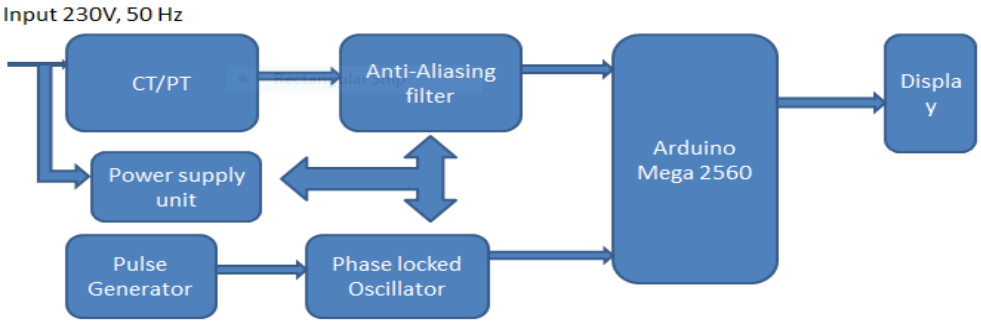

Fig. 4. Block diagram of Laboratory PMU.

The input is taken from 230 V, 50 Hz AC source across which a resistive load is connected. The voltage is stepped down by a P.T (see abbreviations) to 6V and fed to Arduino Mega after passing through a bridge rectifier. The current signal is stepped down by C.T and converted to voltage signal by connecting resistor of calculated value across it and further passed through anti-aliasing filter. The output is fed as analog signal to Arduino. The sampling frequency is given by phase locked oscillator which takes its input from pulse generator generating pulses of 100 Hz. All three inputs, which is voltage signal, current signal and sampling signal are fed to Arduino which carries out phasor estimation with the use of DFT technique. The output is displayed in MATLAB software.

Input supply and signalling: Input to the Laboratory PMU is taken from domestic single phase supply of 230 V, 50 Hz across which a resistive load is connected. In parallel connection, the same supply is fed to the potential transformer (PT) to step down the voltage from 220V to 6V to obtain voltage signal for processing. To obtain current signal, the neutral wire (black) is passed through the centre of current transformer(CT). Input supply to load and then to PT and CT for signalling of laboratory PMU is shown in Fig. 5-7.

Fig. 5. Input to the resistive load.

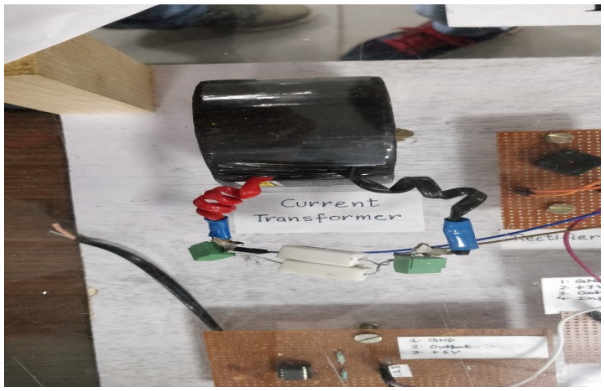

Fig. 6. Current Transformer.

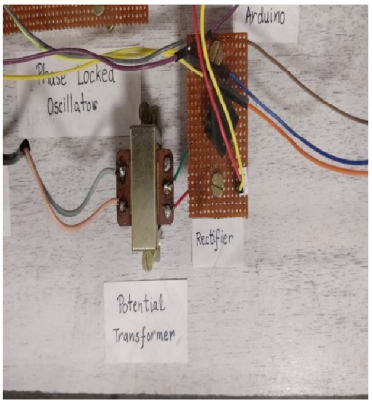

Fig. 7. Potential Transformer.

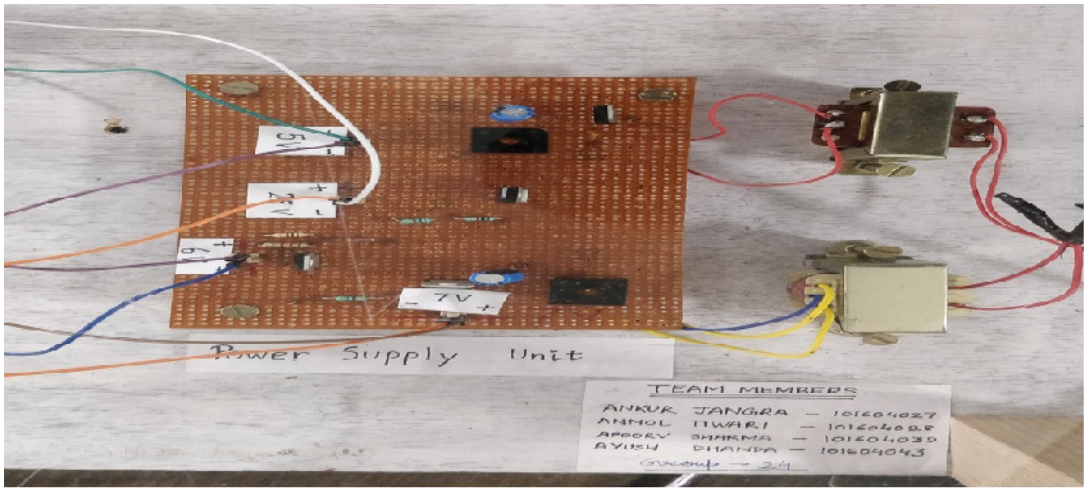

Fig. 8. Power supply unit.

Power supply unit: The power supply unit which is used to power different ICs used in the various units like anti-aliasing filter, pulse generator and phase locked oscillator and also to power Arduino board. The hardware design of power supply unit is presented in Fig. 8.

It includes the following components:

— Two step down transformers ratings 6-0-6 and 12-0-12 to step down voltage to 6V and 12V respectively.

— LM 317- Variable voltage regulator- It is used to give output voltage 2.5V, 5V and 9V to power ICs of anti-aliasing filter and phase locked oscillator respectively. Two such devices are USED.

Anti-Aliasing filter: The hardware design of anti-aliasing filter is shown on Fig. 9.

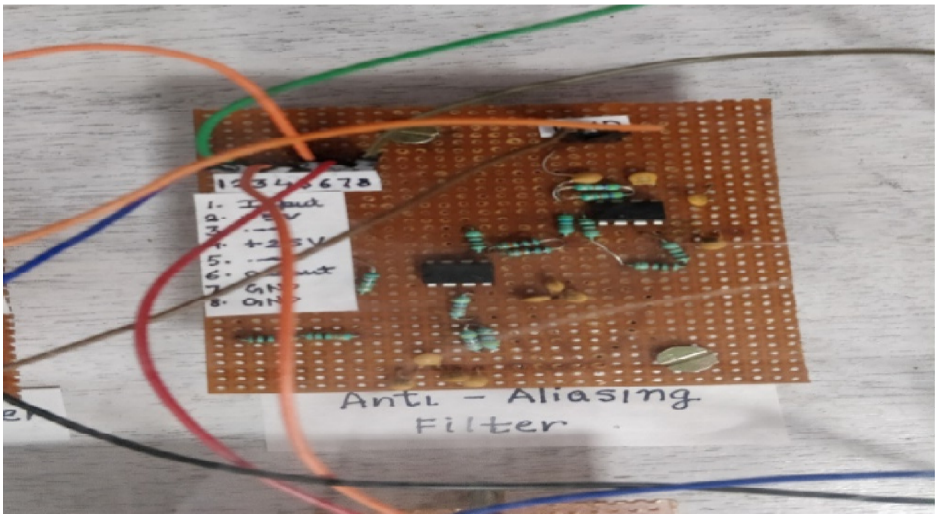

Fig. 9. Anti-Aliasing filter.

It includes the following components:-
— LM 741- Operational amplifier IC- 2 units
— Resistors and capacitors
Pin number 2 and 3 of Op-Amp are non-inverting and inverting inputs respectively. The ground is connected to pin number 4. The output is taken from pin number 6. A feedback capacitance of 910pf is connected across 3 and 6. The supply to the IC is given to pin number 7.

Pulse generator: The input to the PLO is given by pulse generator which gives pulses of 100Hz. The hardware design of pulse generator is given in Fig. 10.

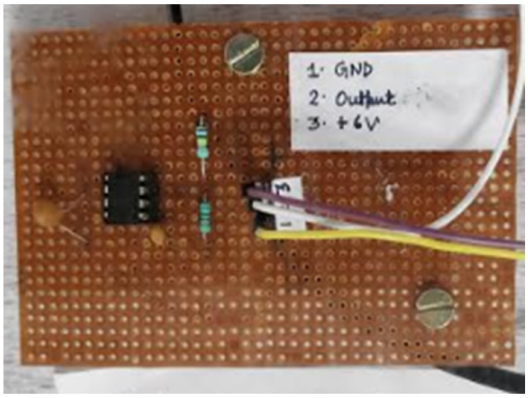

Fig. 10. Pulse generator.

It uses a timer IC 555 which is an Astable multivibrator generating pulses of the required frequency of 100Hz. The hardware design of phase locked oscillator is given in Fig. 11.

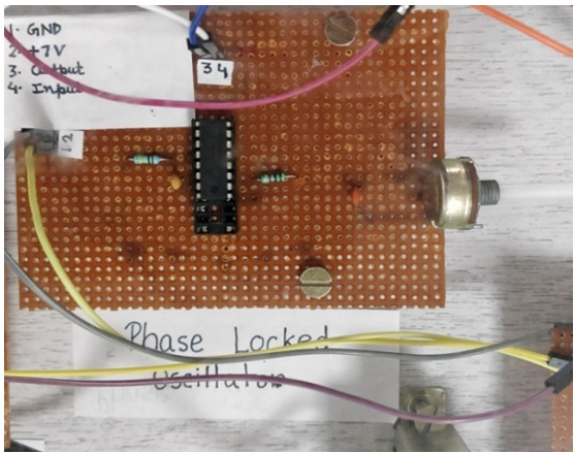

Fig. 11. Phase locked oscillator.

Phase locked Oscillator: Hardware of PLO consists of PLL IC 4046 along with feedback resistors and capacitors of desired values. A potentiometer of 50k ohm is connected to give the variable frequency output. PLO receives 100 Hz signal from pulse generator as input and gives pulses of frequency up to 80 kHz (tested) as output.

Arduino Mega 2560: The connection to Arduino from various units for phasor estimation of incoming signals is shown in Fig. 12.

The three inputs fed to the Arduino are fed as analog signal to the pin numbers A2, A4, A6. The inputs are acquired by MATLAB from Arduino through Arduino support package library. The signals are processed in MATLAB environment and displayed in the software itself.

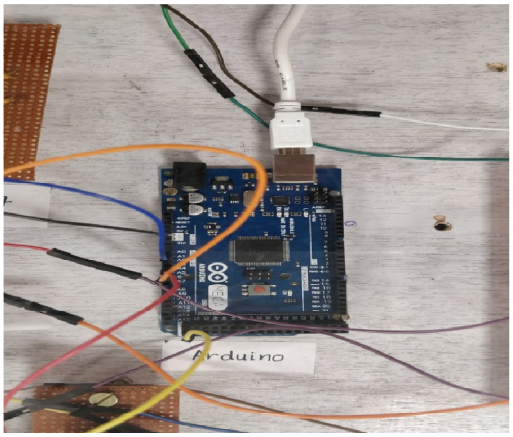

Fig. 12. Arduino Mega 2560.

Laboratory PMU: The following Fig. 13 shows the integrated hardware design of Laboratory PMU.

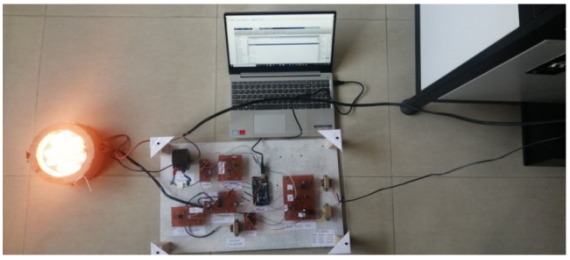

Fig. 13. Laboratory PMU.

Mathematical Calculations

Power supply unit

The output voltage of LM 317 is given by the formula

$V_{out} = 1.25*(1+(R_2/R_1))$ (6)

For output voltage of 2.5 V

$V_{out} = 1.25*(1+(1000\Omega/1000\Omega))$

$= 2.5$ V

For output voltage of 5 V

$V_{out} = 1.25*(1+(3000\Omega/1000\Omega))$

$= 5$ V

For output voltage of 9V

$V_{out} = 1.25*(1+(6200\Omega/1000\Omega))$

$= 9$ V

Anti-Aliasing filter

Determination of cut-off frequency

$F_c = (1/(2*\pi*R*C))$ (7)

Where R= resistor value

C= feedback capacitor

$F_c = 1/(2*\pi*910*10^{-9}F*10^5\Omega)$

$= 54.94$ Hz

Phase locked oscillator

The output frequency of pulse generator is given by

$F_{out} = 1/(R*C)$ (8)

$= 1/(100*10^3*0.1*10^{-6}F)$

$= 100$ Hz.

The output frequency of PLO corresponding to input of 100Hz is given by

$F_{out} = 0.25/(R_v*C_v)$ (9)

For maximum value of R= 50kΩ

$F_{out} = 80$ kHz

IV. RESULTS AND DISCUSSION

Simulation Results of Anti-Aliasing Filter: The frequency response of the anti-aliasing filter during its software implementation is shown in Fig. 14. It has been observed that the filter gives flat response up to the cut-off frequency of 54.94 Hz and attenuates the signal above this frequency.

Simulation Results of Phase locked oscillator: Fig. 15 depicts the result obtained after software implementation of phase-locked oscillator in PROTEUS environment. It has been observed that 80kHz sampling pulses of amplitude 860 mV peak to peak are generated for 1 PPS input signal.

Implementation of Anti-Aliasing filter: The output of anti-aliasing filter is shown in Fig. 16 which has taken input voltage signal consisting of fundamental frequency and noises corresponding to the current signal that appears at the output of CT during its hardware implementation. It has been found that only fundamental frequency components are present at the output of anti-aliasing filter.

Implementation of Phase locked oscillator: The phase locked oscillator has given sampling pulses of frequency 80 kHz for 100 Hz input signal as can be seen in Fig. 17.

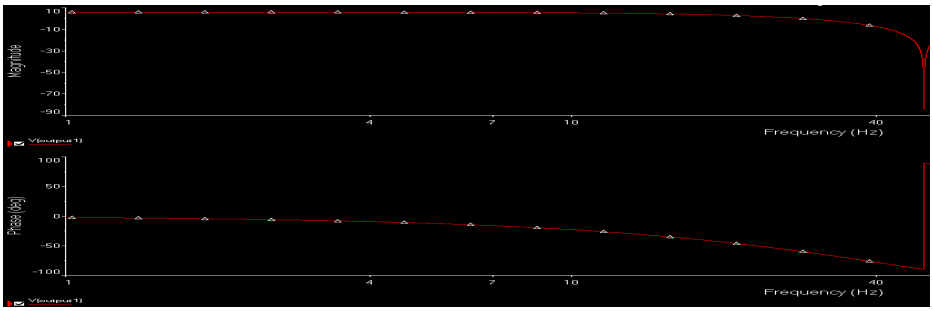

Fig. 14. Frequency response of anti-aliasing filter.

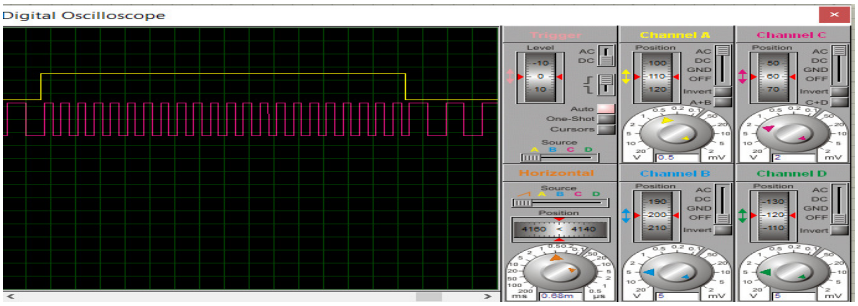

Fig. 15. Simulation result of phase locked oscillator.

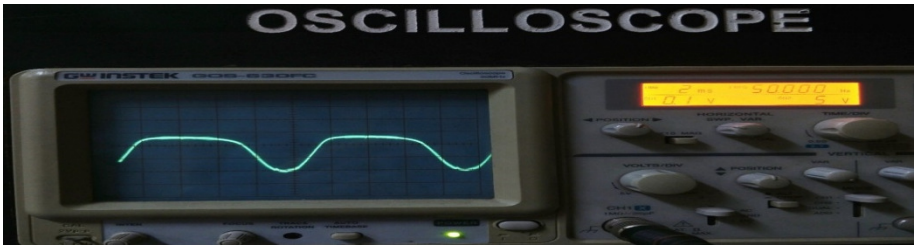

Fig. 16. Hardware result of anti-aliasing filter.

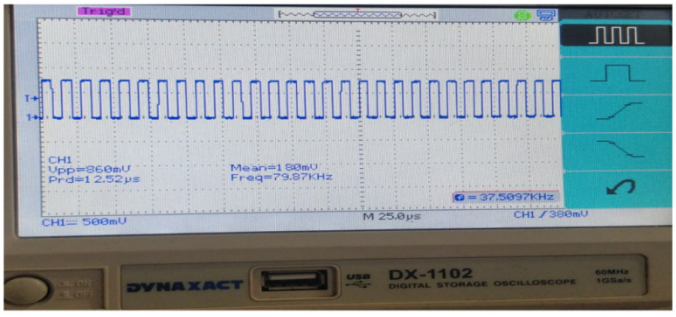

Fig. 17. Hardware result of phase locked oscillator.

Phasor Measurements: The Fig. 18 presents the voltage signal acquired in MATLAB environment through Arduino-Mega 2560. It has been found that the peak value of voltage signal is 4.89 V.

The voltage corresponding to the current signal acquired in MATLAB environment through Arduino-Mega 2560 has been shown in Fig. 19.

The Figs. 20 and 21 presents the voltage phasor measurement using DFT phasor measurement technique for different number of samples (N) such as 960,1400 and 3500. It has been observed that the peak value of measured voltage approaches to theoretical value as the number of samples increases.

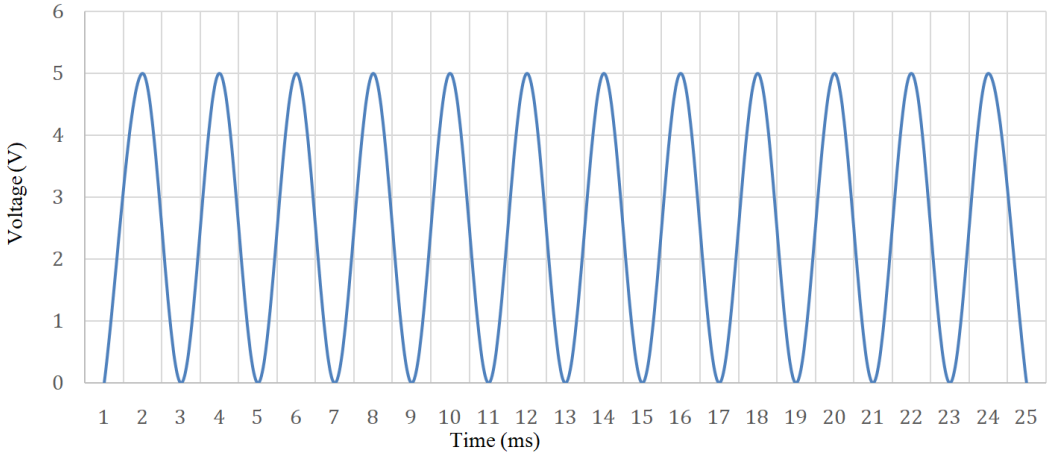

Fig. 18. Input Voltage signal.

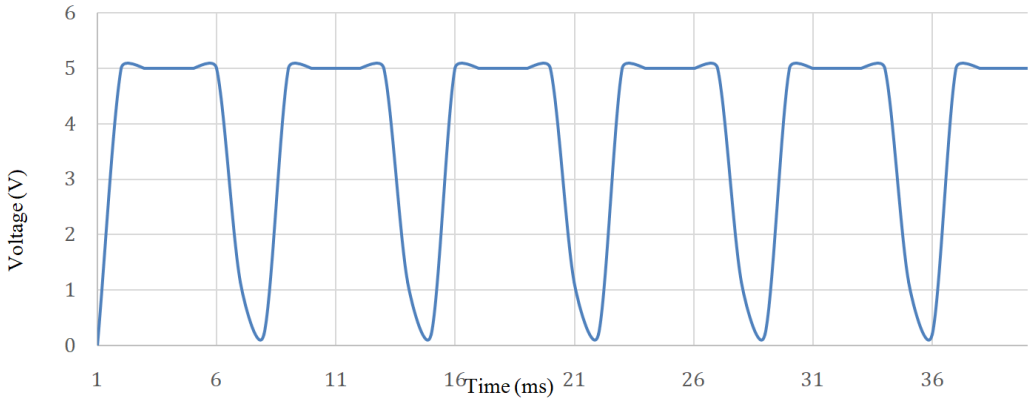

Fig. 19. Input Voltage corresponding to Current signal.

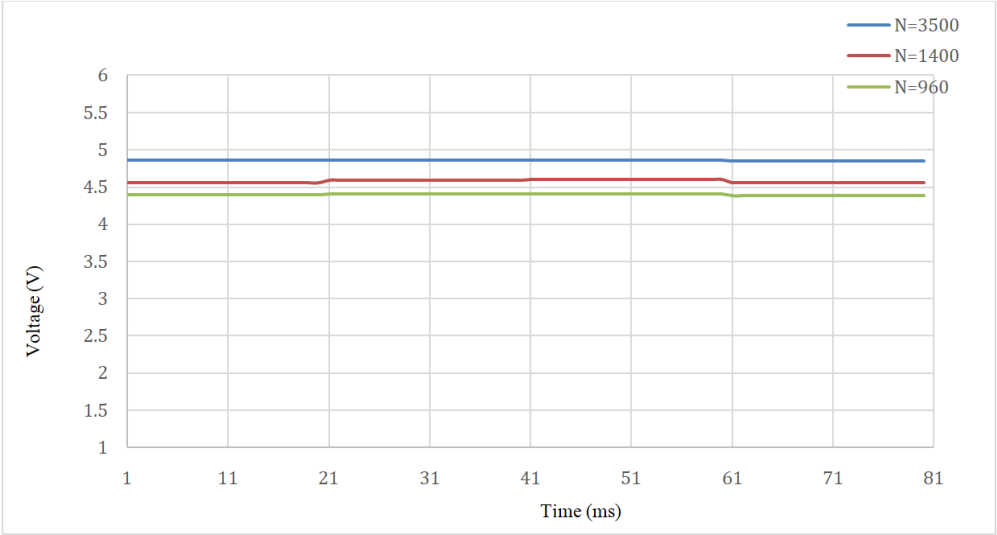

Fig. 20. Measured Voltage Magnitude.

The phasor measurement of voltage corresponding to the current signal using DFT phasor estimation technique for different number of samples (N) such as 960, 1400 and 3500 is shown in Fig. 22 and 23.

Table 1 shows the comparison of theoretical and measured values of voltage corresponding to current and voltage for different values of number of samples. The total vector error corresponding to each measurement is also mentioned.

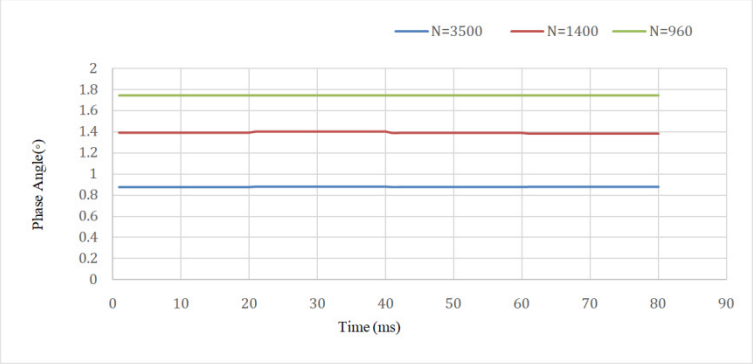

Fig. 21. Measured Voltage Phase angle.

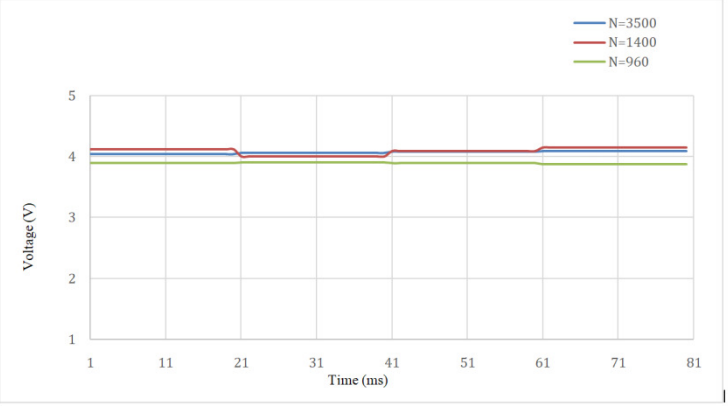

Fig. 22. Measured Voltage corresponding to the current signal.

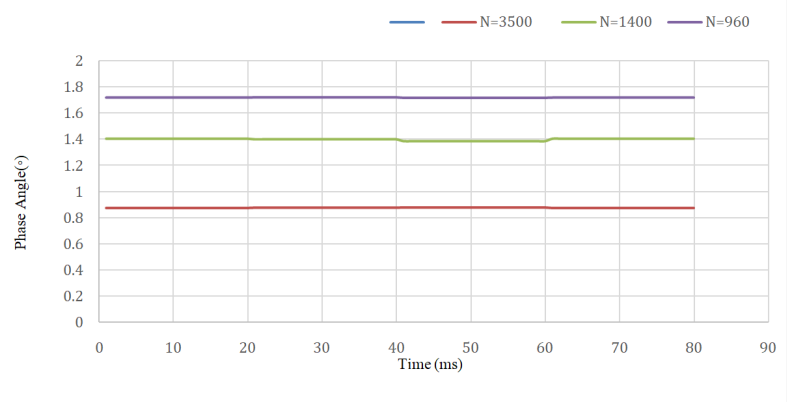

Fig. 23. Measured Phase angle.

Table 1: Comparison of theoretical and measured values.

Signal	Number of samples	Theoretical value	Measured value	Total Vector Error
Voltage	960	4.43 V	4.3933 V	0.97 %
	1400	4.56 V	4.532 V	0.82 %
	3500	4.89 V	4.8582 V	0.65 %
Voltage corresponding to Current	960	3.90 V	3.8374 V	1.8 %
	1400	4.16 V	4.1141 V	1.2 %
	3500	4.07 V	4.0359 V	0.96 %

It can be clearly observed from Table 1 that as the number of samples increases TVE decreases and the measured value approaches to theoretical value which is measured using digital multimeter.

V. CONCLUSION

Following facts and observations can be concluded from the proposed laboratory PMU:

— Analog Butterworth filter of 4^{th} order has been used to function as Anti-Aliasing filter as it provides the desired frequency response.

— Current signal was needed to pass through anti-aliasing filter as it contains noise whereas voltage signal has been directly fed for processing.

— Class 1 CT has been very well used for signalling of PMU.

— Variable frequency voltage-controlled oscillator is used as Phase locked oscillator whose output frequency can be varied by changing the value of feedback resistor.

— Arduino Mega 2560 board has been used for DFT based phasor estimation with ease.

— The results obtained were in compliance with the IEEE standard C-37.118 which states TVE to be less than 1% .

It can also be concluded that the phase angle difference between the voltage and current signal was found to be negligible for a resistive load hence verifying the theoretical concept.

VI. FUTURE SCOPE

In future work, more efficient techniques such as TWLS and SDFT can be used for better phasor estimation. The sampling rate can be further increased for better accuracy. Modern microcontroller like Texas Instruments based TIVA C series which uses ARM based technology for synchronous data acquisition can be used for better data communication synchronization between processing and monitoring devices. As Arduino's application is limited in areas where parallel communication required, thus modern technologies can be incorporated for parallel computation.

Conflict of interest. The authors declares no conflict of interest.

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