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Simulation of Self-balanced based Step-Up Switched Capacitor Nine Level Inverter with MCPWM Scheme

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ABSTRACT: The switched capacitor based nine-level step-up inverter with self-balancing method is presented in this article. The objective of the presented topology is to convert DC into AC by boosting the voltage without any converter, transformers. The single DC source is initiated as an input to the system. The capacitors are connected in parallel and series for charging and discharging respectively. The energy of the capacitors is utilized by the self-balancing method. The voltage stress across the switches are same in this topology. The carrier-based phase disposition PWM technique is used for the switching pulses. Due to not having any H-bridges, the switching and conduction losses are less in this topology, and hence the efficiency is more. The comparative analysis is made between proposed inverter topology with existing topologies in terms of voltage stress, switches and TVS. The practical implementation of the proposed topology is done by using MATLAB/SIMULINK.

Keywords: Self-balancing, Boost, Switched capacitors, Total Voltage stress, Peak Inverse Voltage, Multi carrier-based PWM.

Abbreviations: DC, direct current; AC, alternating current; PWM, pulse width modulation; PIV, peak inverse voltage; TVS, total voltage stress. .

I. INTRODUCTION

The usage of Multilevel Inverters is increasing rapidly for high power energy conversion systems [1]. The general function of multilevel inverters is the conversion of DC into AC [2]. These produce staircase waveforms from power semiconductor devices, DC sources, and diodes. Renewable sources, fuel cells, batteries can be used as different input sources to the multilevel inverters [3]. The Multilevel Inverters have advantages such as low harmonics, low voltage stress, low common-mode voltage, and low distortion input current [4]. Grid-connected systems, Electric vehicles, induction heating are some of the applications of Multilevel Inverters [5]. Classically, the Multilevel Inverters are of three types [6], namely, Neutral Point Clamped (NPC), Flying Capacitors (FC), and Cascaded H-Bridge (CHB). The NPC can produce multilevel output with semiconductor switches, diodes, and capacitors. The major problems in NPC, it requires several diodes to produce high level, the voltage sharing is unequal in the capacitors which lead to high current, high switching losses [7]. The CHB inverters need a high number of H-Bridge converters for the high level of output along with separate DC sources for each unit [8]. It requires less number of switching devices compared to NPC, FC inverters. The CHB inverters will be used as symmetrically with equal input sources, and asymmetrically with unequal input sources [9]. Generally, for low DC to high ac applications the transformers, converters, and inductors are involved in many topologies to boost the low voltage to high voltage, which causes the system bulky and expensive [10]. The transformer-less topologies are introduced to boost the system voltage [11]. For high levels of output, several switches, DC sources are required which leads to system complexity, raise in voltage stress and EMI increases [12].

Many researchers are working on the drawbacks of the classical topologies of multilevel inverters and introduced new topologies based on the applications [13]. The new topologies are evolved based on the count of semiconductor switches, total voltage stress capacity, switching frequency, and chances of inserting symmetrical and asymmetrical sources [14]. The Switched Series Parallel Sources (SSPS) multilevel inverter [15], the DC voltage sources are connected in series and parallel with the switches. For high levels of output, the DC voltage sources are additively combined and operated in series and parallel by the switching devices. These can be utilized with symmetrical and asymmetrical sources. The voltage stress across the switches are different, this may lead to high total stress voltages and high THD. The Switched DC source inverters [16], alternatively the input DC supplies are connected their polarities in reverse through the switches. Compared to classical topologies, the number of semiconductor switches are less in Switched DC source inverters. It is used for medium voltage drive applications, battery-powered applications especially in

electric vehicles, marine propulsion. The Packed U-cell (PUC) inverters [17], evolves a self-voltage balancing process to obtain high levels of output. The capacitor rating is keep fixed which is equal to half of the magnitude of input DC sources. The switched capacitor inverters [18] with H-bridge configuration also have high TVS and PIV.

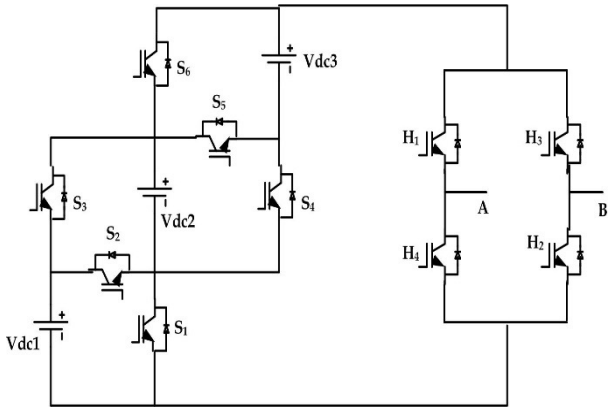
A new type of step-up, self-balanced switched-capacitor nine-level inverter without H-bridge configurations is proposed. It comprises the single DC input source, power switches, and capacitors. The carrier-based phase disposition PWM scheme is utilized for this proposed topology. The capacitors will be charged and discharged by the self-balancing process. Due to the self-balancing process, the voltage stress across the switches is the same, equals to the value of the input DC voltage V_{DC}. In this topology, the low input voltage is also boosted to the high output voltage without any converters and transformers by maintaining low TVS and PIV of the system.

II. PROPOSED TOPOLOGY AND OPERATING STATES

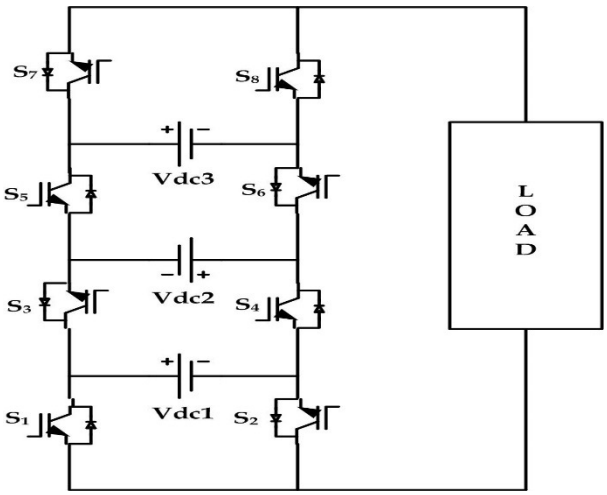
A. Basic Proposed Module

The basic proposed topology module is displayed in Fig. 2. The basic module resides the DC voltage source, five semi-conductor switches, and a capacitor. The input excitation to the proposed method will be given from fuel cells, batteries, PV module, etc.

Initially, when the DC input voltage is applied, the capacitor has to be charged fully through the switches Spa_3, Spa_2, and the capacitor voltage is equivalent to the applied DC voltage as shown in Fig. 2(a). The charged capacitor will be discharged positively and negatively through the switches Spa_2, Spa_5, and Spa_1, Spa_4 respectively as shown in Fig. 2(b). The switches Spa_1, Spa_2, and Spa_4, Spa_5 are operated complimentary during discharging in positive and negative paths.



(a)



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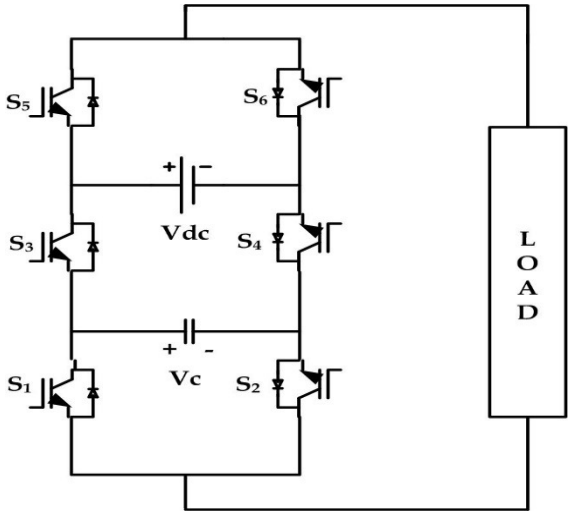

(c)

Fig.1. (a). SSPS [15], (b) Switches DC Sources [16], (c) PUC [17].

B. Proposed Switched-Capacitor Topology

The cascaded connection of three basic modules forms the proposed topology to produce nine-level output is shown in Fig. 3. The three switched capacitors are placed in parallel with the input DC supply. Without boost converter, transformers, inductors the input voltage is boosted up by using self-balancing process. First, the three capacitors have charged completely which is equal to the input voltage V_{DC}. The charged capacitors will generate the levels and step-up the voltages. During charging of the capacitors, the output voltage will be zero. The capacitors charging state is given in Fig. 4.

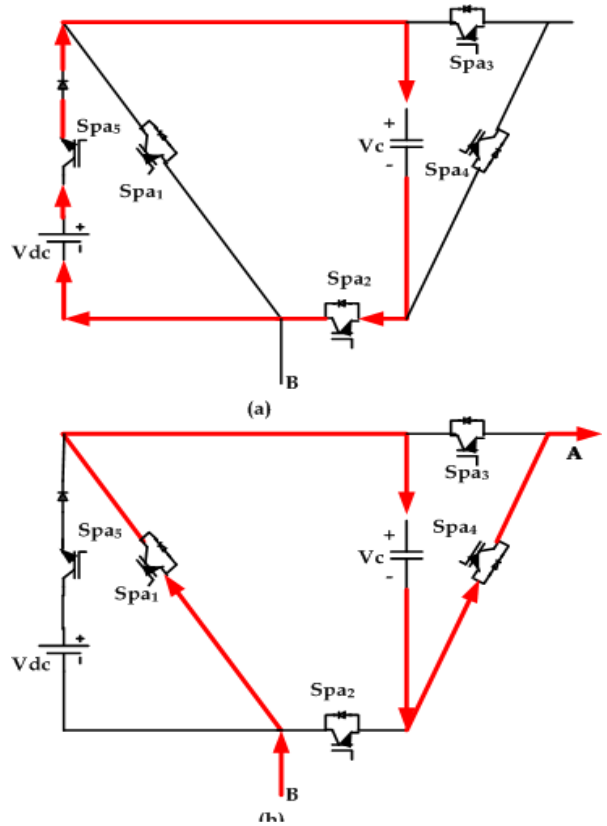

Fig. 2. Basic Module of proposed topology, (a) Charging state, (b) Discharging state.

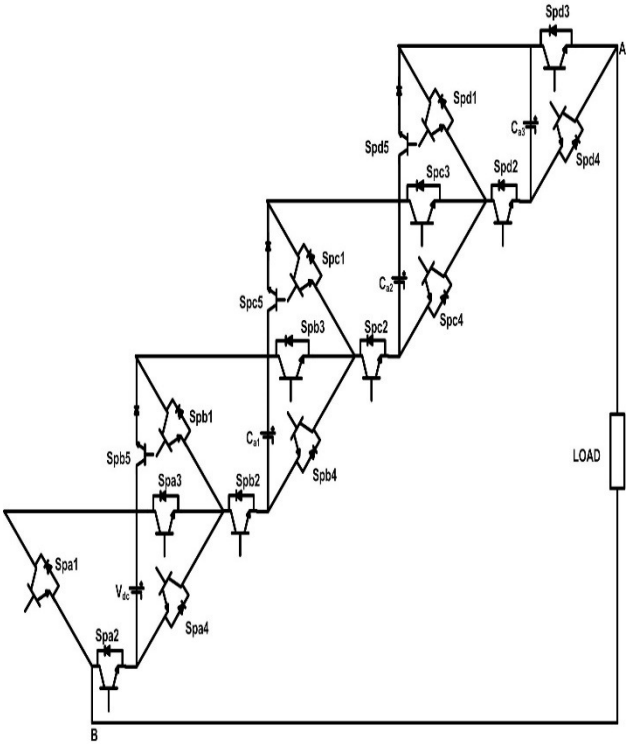

Fig. 3. Proposed Switched-Capacitor Inverter Topology.

During charging state of the capacitor, the voltage across the capacitors is normally given as

$$V_{Can\ (charging)}\ (t) = V_{in}\ C_{an}\ (1 - e^{\frac{-t}{\tau Can}}) \quad (1)$$

Where $V_{in\ Can}$ is the capacitor's input voltage, τ_{Can} is the capacitor's time constant. The capacitor voltages V_{Can} is depended on the conduction switches resistances $R_{sw,on}$, diode resistancnes $R_{d,on}$, conduction switches voltage drops $V_{sw,on}$, and diode's voltage drops $V_{d,on}$. During the charging of capacitor C_{a1}, two semi-conductor switches Spb_5, Spa_4, two diodes will conduct and the capacitor C_{a1} will charge to $1V_{DC}$. Four semiconductor switches Spb_5, Spc_5, Spb_4, Spa_4, four diodes will conduct for the charging of capacitor C_{a2}. For the charging of capacitor C_{a3}, six semiconductor switches Spb_5, Spc_5, Spd_5, Spc_4, Spb_4, Spa_4, six diodes are in ON-state. The three capacitor voltages in the charging state are represented as.

$$V_{Ca1\ (charging)}\ (t) = \left[V_{DC} - \left(2V_{sw,on} + 2V_{d,on} + (2(R_{sw,on} + R_{d,on}) + r_{ca1})\, i_{ca1v}\right]\left(1 - e^{\frac{-t}{(2(R_{sw,on}+R_{d,on})+r_{ca1})\, c_{a1}}}\right) \quad (2)$$

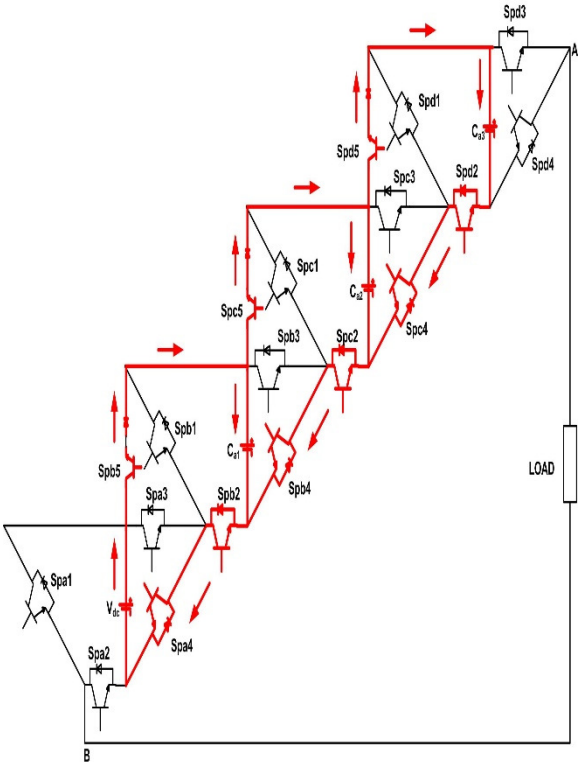

Fig. 4. Charging state of Proposed Inverter.

$$V_{Ca2\ (charging)}\ (t) = \left[V_{DC} - \left(4V_{sw,on} + 4V_{d,on} + (4(R_{sw,on} + R_{d,on}) + r_{ca2})\, i_{ca2v}\right]\left(1 - e^{\frac{-t}{(4(R_{sw,on}+R_{d,on})+r_{ca2})\, c_{a2}}}\right) \quad (3)$$

$$V_{Ca3\ (charging)}\ (t) = \left[V_{DC} - \left(6V_{sw,on} + 6V_{d,on} + (6(R_{sw,on} + R_{d,on}) + r_{ca3})\, i_{ca3v}\right]\left(1 - e^{\frac{-t}{(6(R_{sw,on}+R_{d,on})+r_{ca3})\, c_{a3}}}\right) \quad (4)$$

C. Discharging states of proposed topology

The fully charged capacitors have to be discharged to produce the desired staircase output voltage waveform in series with different levels at desired frequency and amplitude. The positive discharging states of topology is shown Fig. 5.For the voltage $+1V_{DC}$, the input voltage

V_{DC}, five switches Spa_3, Spb_2, Spc_2, Spd_2, Spa_2 and three diodes will conducts which is shown in Fig. 5(a).The capacitor C_{a1} will starts to discharge through the six switches Spa_3, Spb_2, Spb_3, Spc_2, Spd_2, Spa_2 along with two diodes for producing $+2V_{DC}$ as shown in Fig. 5(b).

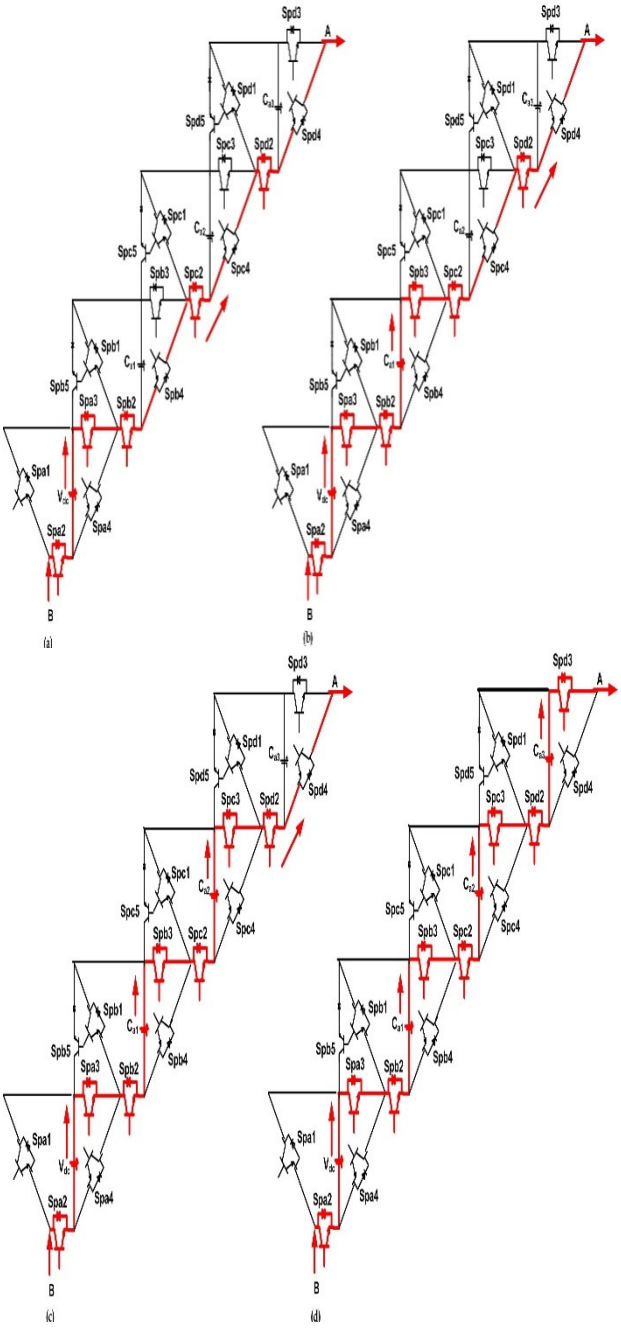

Fig. 5. Discharging positive states: (a) $+1V_{DC}$ (b) $+2V_{DC}$ (c) $+3V_{DC}$ (d) $+4V_{DC}$.

For $+3V_{DC}$, the capacitor C_{a2} is added with capacitor C_{a1} to discharge through Spa_3, Spb_2, Spb_3, Spc_2, Spc_3, Spd_2,Spa_2 switches, a diode as shown in Fig. 5(c). From Fig. 5(d) shows the producing of $+4V_{DC}$ output voltage by discharging of three capacitors C_{a1}, C_{a2}, C_{a3} through the eight conducting switches Spa_3, Spb_2, Spb_3, Spc_2, Spc_3, Spd_2, Spd_3, Spa_2. However, the number of conducting switches is different for each level of output voltage but, the voltage stress across the each switch is same.

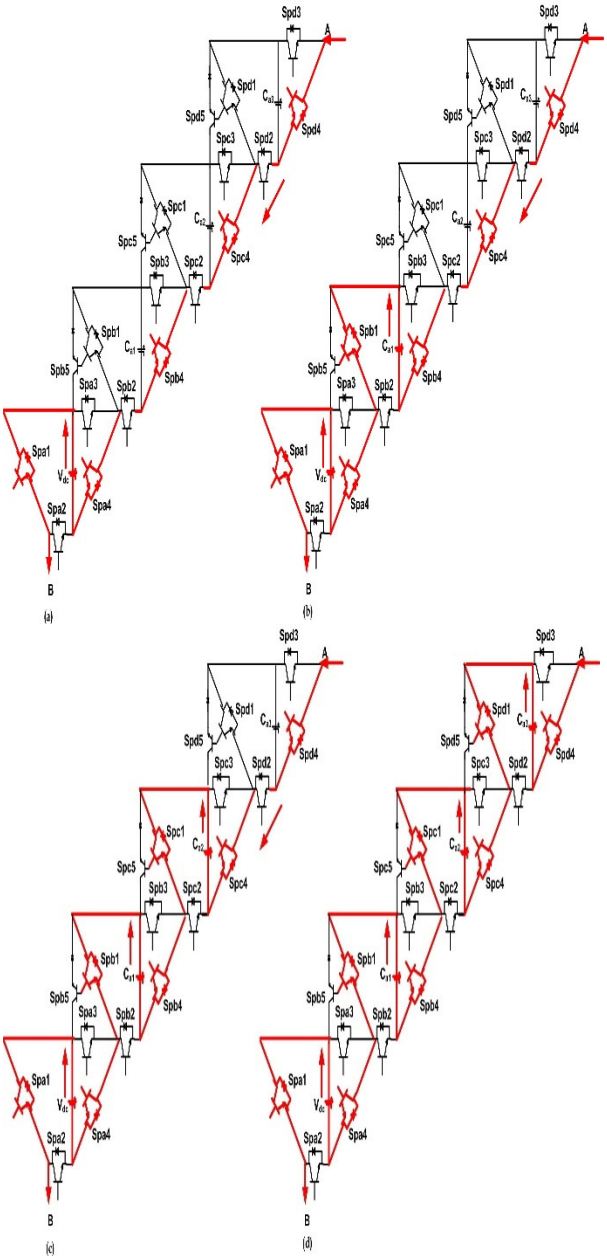

Fig. 6. Discharging negative states: (a) $-1V_{DC}$ (b) $-2V_{DC}$ (c) $-3V_{DC}$ (d) $-4V_{DC}$.

The complemental operation of positive discharging state gives the negative discharging state as shown in Fig. 6. The switches Spa_1, Spd_4, Spc_4, Spb_4, Spa_4 will conduct for the producing the $-1V_{DC}$ which is shown in Fig. 6(a). The capacitor C_{a1} discharges in a negative direction through the switches Spa_1, Spd_4, Spc_4, Spb_4, Spb_1, Spa_4 for producing $-2V_{DC}$ output voltage level is shown in Fig. 6(b). From Fig. 6(c), the two capacitors C_{a1}, C_{a2} are connected in series, discharges through the

switches Spa_1, Spd_4, Spc_4, Spc_1, Spb_4, Spb_1, Spa_4 to produce $-3V_{DC}$ voltage level. The three capacitors C_{a1}, C_{a2}, C_{a3} are discharging in series through the switches Spa_1, Spd_4, Spd_1, Spc_4, Spc_1, Spb_4, Spb_1, Spa_4 for $-4V_{DC}$ voltage level as shown in Fig. 6(d).

III. MODULATION SCHEME

The multi carrier-based modulation control scheme is involved for the proposed switched capacitor nine-level inverter presented in Fig. 7. The carrier signal has eight triangular signals with 50KHz frequency is compared with the reference sinusoidal signal of 50Hz frequency to create the switching pulses to the inverter. From Fig. 7, four triangular carrier signals c_1, c_2, c_3, c_4 are used to produce positive voltages, other four carrier signals c_5, c_6, c_7, c_8 are producing negative voltages.

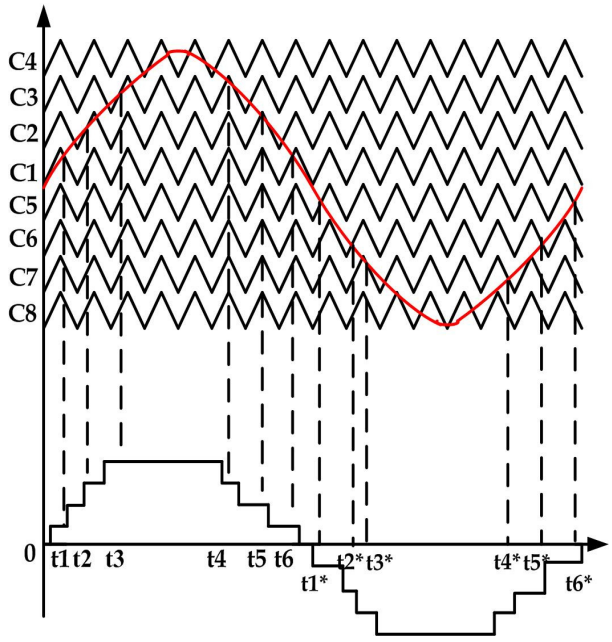

Fig. 7. Multi carrier based PWM.

The time instants to produce nine-level output is given as

$$t_i = \frac{\sin^{-1}\left(\frac{A_{ci}}{A_r}\right)}{2\pi f_r} \quad (5)$$

where, i = time instants 1,2,3….

$$t_1 = \frac{\sin^{-1}\left(\frac{1}{A_r}\right)}{2\pi f_r} \quad (6)$$

$$t_2 = \frac{\sin^{-1}\left(\frac{2}{A_r}\right)}{2\pi f_r} \quad (7)$$

$$t_3 = \frac{\sin^{-1}\left(\frac{3}{A_r}\right)}{2\pi f_r} \quad (8)$$

$$t_4 = \pi - t_3 \quad (9)$$

$$t_5 = \pi - t_2 \quad (10)$$

$$t_6 = \pi - t_1 \quad (11)$$

For A_r = 3.9, f_r = 50Hz, the time instants for nine-level output will be calculated. The period t_1 - t_6 is the discharging time of capacitor C_{a1}. From the time t_2 - t_5, the capacitor C_{a2} will be discharged. The discharging period of capacitor C_{a3} is t_3 - t_4. Out of these three capacitor discharging periods, the capacitor C_{a1} has maximum discharging time. By choosing the proper capacitor value, the ripples in the capacitor voltages will be reduced. The capacitor value depends on the amount of maximum discharge, load current and ripple ratio.

The maximum discharging of the capacitor is given as

$$Q_{cai} = \int_{t_{pi}}^{t_{qi}} i_l \sin(\omega_r t) dt \quad (12)$$

The capacitor value is given as

$$Q_{cai} \propto C_{ai} V_{DC} \quad (13)$$

$$Q_{cai} = k_c C_{ai} V_{DC} \quad (14)$$

$$\boldsymbol{C_{ai}} = \frac{\boldsymbol{Q_{cai}}}{\boldsymbol{k_c C_{ai}}} \quad (15)$$

where, k_c =0.3 = ripple constant of the capacitor, t_{pi}, t_{qi} are the starting time, a maximum discharging period of the i^{th} capacitor respectively. The operating states of capacitors, switches, diodes at different time instants are given in Table.1.

IV. SIMULATION RESULTS

In SSPS topology [15], the voltage stress of switches S_2, S_5 is shown in Fig. 8, for input voltage V_{DC1} = V_{DC2} = 100V. The voltage stress of switches S_2, S_5 is 200V, 100V respectively.

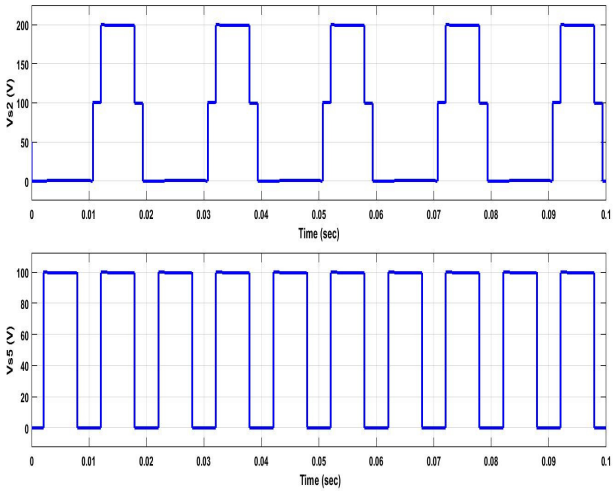

Fig. 8. Voltage stress of switches of SSPS.

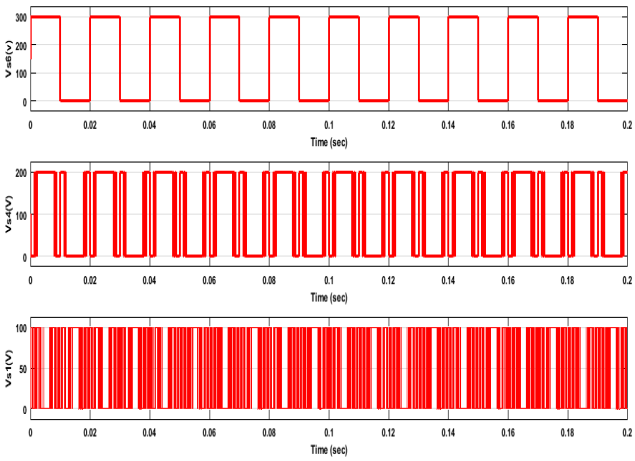

Fig. 9. Voltage stress of switches of Switched DC Sources Inverter.

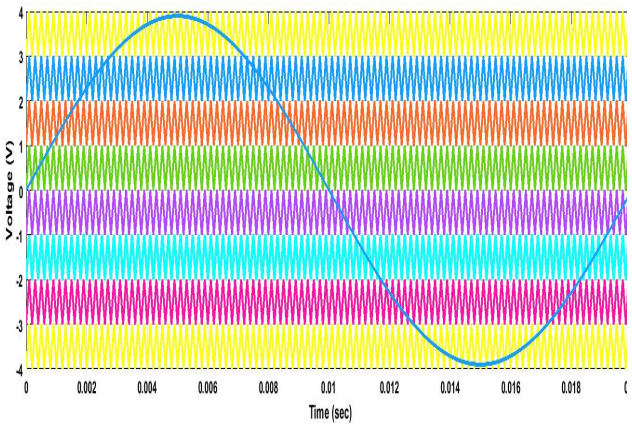

Fig. 10. Carrier-based PWM scheme.

Due to having additional H-bridge configuration, the voltage stress across the switches are not same, which causes high Total Voltage Stress (TVS), high PIV, and high conduction losses. Similarly, the voltage stress of switches of switched DC sources inverter [16] is shown in Fig. 9.

The parameter table for simulation of proposed switched-capacitor inverter topology for producing nine-level output waveform is specified in Table 2. The multi carrier-based based PWM scheme is evolved for the generation of gate pulses. The amplitude of reference sinusoidal signal 3.9 at 50Hz frequency is compared with the amplitude of eight carrier signals at 50KHz frequency to generate pulses is shown in Fig. 10, the PWM pulses are applied to the switches to obtain nine-level output voltage.

Table.1: The different States of Switches, Diodes, and Capacitors.

Time Instants	Conduction Diodes of switches	Conduction Switches	State of Capacitors			V_{out}
			C_{a1}	C_{a2}	C_{a3}	
$t_6 - t_1^*$	Spb_2, Spc_2, Spd_2	Spa_4, Spb_4,Spb_5, Spc_4, Spc_5, Spd_4, Spd_5	C	C	C	0
$0 - t_1$	Spb_4, Spc_4, Spd_4	Spa_3, Spb_2, Spc_2, Spd_2, Spa_2	I	C	C	$+1V_D$ C
$t_1 - t_2$	Spc_4, Spd_4	Spa_3, Spb_2, Spb_3, Spc_2, Spd_2, Spa_2	DC	C	C	$+2V_D$ C
$t_2 - t_3$	Spd_4	Spa_3, Spb_2, Spb_3, Spc_2, Spc_3, Spd_2, Spa_2	DC	DC	C	$+3V_D$ C
$t_3 - t_4$	---	Spa_3, Spb_2, Spb_3, Spc_2, Spc_3, Spd_2, Spd_3, Spa_2	DC	DC	DC	$+4V_D$ C
$t_1^* - t_2^*$	---	Spa_1, Spd_4, Spd_1, Spc_4, Spc_1, Spb_4, Spb_1, Spa_4	DC	DC	DC	$-4V_{DC}$
$t_2^* - t_3^*$	Spd_2	Spa_1, Spd_4, Spc_4, Spc_1, Spb_4, Spb_1, Spa_4	DC	DC	C	$-3V_{DC}$
$t_3^* - t_4^*$	Spc_2, Spd_2	Spa_1 Spd_4, Spc_4, Spb_4, Spb_1, Spa_4	DC	C	C	$-2V_{DC}$
$t_4^* - t_5^*$	Spb_2, Spc_2, Spd_2	Spa_1, Spd_4, Spc_4, Spb_4, Spa_4	I	C	C	$-1V_{DC}$

C = Charging, DC = Discharging, I = Ideal

Table 2: Simulation parameters for the proposed topology.

V_{DC}	100 V
Capacitors (C_{a1}, C_{a2}, C_{a3})	4700μF each
Resistance	50Ω
Inductance	10mH
Reference Frequency (f_r)	50Hz
Carrier Frequency (f_c)	50KHz
Switch ON state resistance ($R_{sw,on}$)	1mΩ

The output voltage 380V and current 7.5A is obtained from the proposed topology by boosting the input voltage 100V without any converters is shown in Fig. 11& Fig. 12.

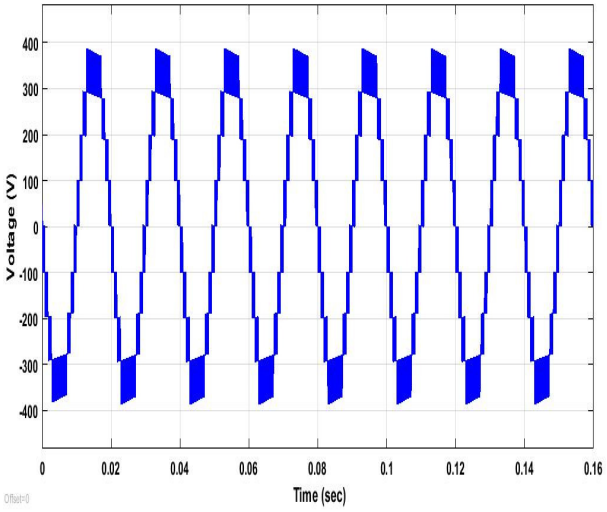

Fig. 11. Output voltage of the proposed topology.

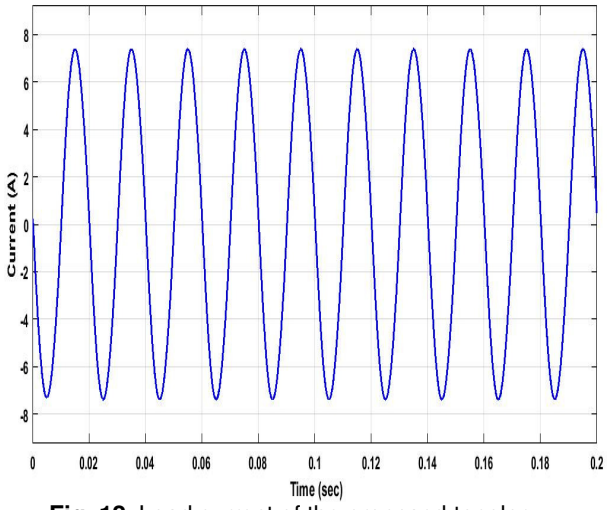

Fig. 12. Load current of the proposed topology.

The three capacitor voltages C_{a1}, C_{a2}, C_{a3} are shown in Fig. 13, with 30% ripple factor having the same voltages. The voltage across each switch in a single module of the proposed switched-capacitor inverter is shown in Fig. 14.

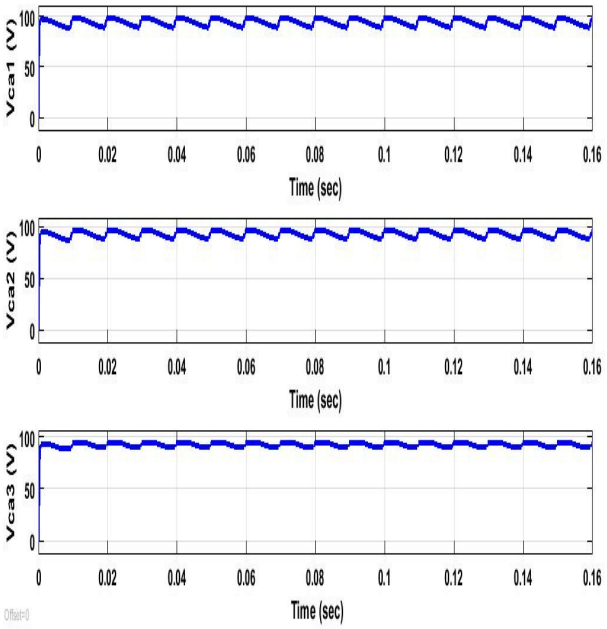

Fig. 13. Capacitor voltages V_{ca1}, V_{ca2}, V_{ca3}.

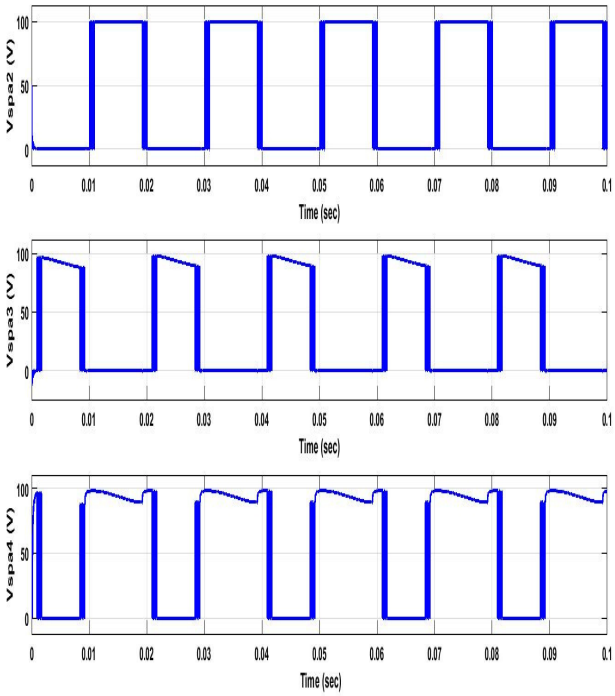

Fig. 14. Voltage stress of switches in the proposed topology.

The voltage stress of each switch is equal to input voltage V_{DC} = 100V by eliminating the H-bridge configuration. Therefore, the total voltage stress of the proposed inverter is very less compared to the existing topologies.

V. COMPARISONS

Table 3 shows the comparison between the proposed switched-capacitor based nine-level inverter and popular existing topologies for 2n+1 level.

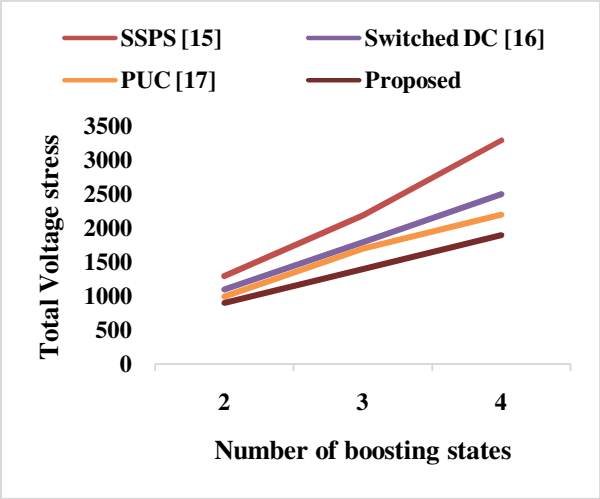

Fig. 15. Comparative analysis of Total Voltage Stress (TVS) between proposed topology and the existing topologies.

The existing topologies SSPS [15], Switched DC sources [16] requires several input sources compared to the proposed topology. The conduction switches voltage stress is very high in existing topologies than the proposed causes high Total Voltage Stress (TVS) as shown in Fig. 15. Even though, the proposed topology requires several semiconductor devices are shown in Fig. 16, the Total Voltage Stress (TVS) is low compared to existing topologies. The proposed topology does not have any H-bridge configuration, so, the PIV is $1V_{DC}$, but for existing topologies the PIV is nV_{DC}.

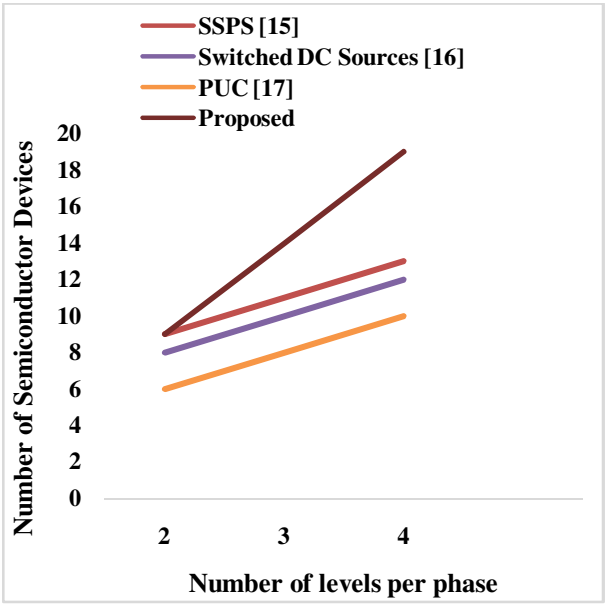

Fig. 16. Comparative analysis of number of semiconductor devices between proposed topology and the existing topologies.

Table 3: Comparative analysis between proposed topology with existing topologies.

	SSPS [15]	Switched DC Source [16]	PUC [17]	Proposed
DC Source	4	4	1	1
Active Switches	3n+1	2(n+1)	3n-2	5n-1
Capacitors	0	0	n-1	n-1
H Bridges	Need	No Need	No Need	No Need
PIV	n V_{DC}	n V_{DC}	n V_{DC}	1 V_{DC}
TVS	(n^2+1+4n) V_{DC}	(7n-3) V_{DC}	(n^2 -2n) V_{DC}	(5n-1) V_{DC}
Complexity	Yes	Yes	Yes	No
Control of Capacitors	--	--	Self-balancing	Self-balancing

VI. CONCLUSION

A self-balanced boost switched capacitor nine-level inverter is simulated using MATLAB/SIMULINK. The proposed topology is not only converting the DC into AC, but also boosting the voltage without any converters and transformers. The charging and discharging states of the proposed inverter by self-balanced process produces the nine-level output voltage. The mathematical representation of charging, discharging, and capacitor capacity is also conducted. The multi carrier-based PWM control scheme is involved to provide switching pulses to the inverter. The comparative analysis between proposed and existing topologies shows the voltage stress of all switches are the same and equals to $1V_{DC}$ in proposed, but not in existing topologies. Therefore, the proposed has low Total Voltage Stress (TVS), low PIV, low conduction and switching losses, modularity, and cost-effective.

VII. FUTURE SCOPE

In future, there is a scope, the proposed self-balanced boost switched capacitor nine level inverter can be used in many applications such as Grid connected RES, Electrical Vehicles etc. It is also possible that, the different modulation techniques can also be applied to this proposed inverter to improve the Total Harmonic Distortion.

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